

Source and Sink, 1.5A, Fast Transient Response Linear Regulator

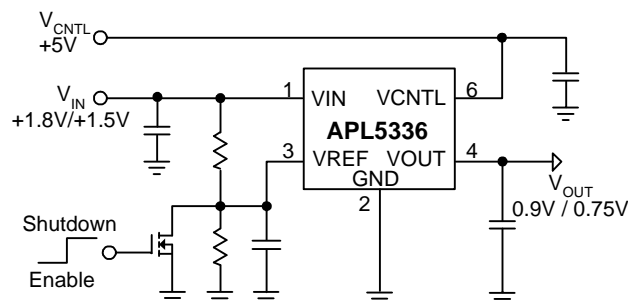
Features

- **Provide Bi-direction Output Currents**
- Sourcing and Sinking Current up to 1.5A
- **Built-In Soft-Start**
- **Power-On-Reset Monitoring on VCNTL and VIN Pins**
- **Fast Transient Response**
- **Stable with Ceramic Output Capacitors**
- **±20mV High System Output Accuracy Over Load and Temperature Ranges**
- **Adjustable Output Voltage by External Resistors**
- **Current-Limit Protection**
- **On-Chip Thermal Shutdown**
- **Shutdown for Standby or Suspend Mode**
- **Simple SOP-8 and SOP-8 with Exposed Pad (SOP-8P) Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **DDRII/III SDRAM Termination Voltage**
- **Motherboard and VGA Card Power Supplies**
- **Setop Box**
- **SSTL-2/3 Termination Voltage**
- **Low Power DDR3**

Simplified Application Circuit



General Description

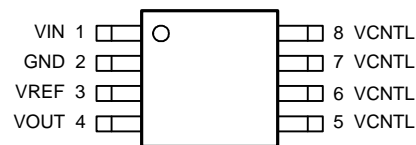
The APL5336 linear regulator is designed to provide a regulated voltage with bi-direction output current for DDR-SDRAM termination voltage. The APL5336 integrates two power transistors to source or sink load current up to 1.5A. It also features internal soft-start, current-limit, thermal shutdown, and enable control functions into a single chip.

The internal soft-start controls the rising rate of the output voltage to prevent inrush current during start-up. The current-limit circuit detects the output current and limits the current during short-circuit or current overload conditions. The on-chip thermal shutdown provides thermal protection against any combination of overload that would create excessive junction temperatures.

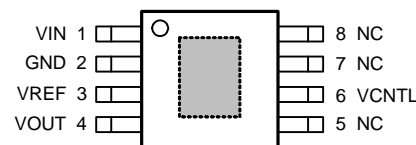
The output voltage of APL5336 is regulated to track the voltage on VREF pin. An proper resistor divider connected to VIN, GND, and VREF pins is used to provide a half voltage of VIN to VREF pin. In addition, connect an external ceramic capacitor and a open-drain transistor to VREF pin for external soft-start and shutdown control.

Pulling and holding the voltage on VREF below the enable voltage threshold shuts down the output. The output of APL5336 will be high impedance after being shut down by VREF or the thermal shutdown function.

Pin Configuration



Top View of SOP-8

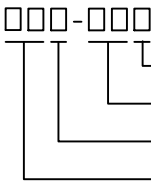

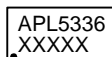


Top View of SOP-8P

 Exposed Pad (connected to GND plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL5336	 <p> Assembly Material Handling Code Temperature Range Package Code </p>	Package Code K : SOP-8 KA : SOP-8P Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL5336 K:		XXXXX - Date Code
APL5336 KA:		XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 7	V
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 7	V
V_{REF}	VREF Input Voltage (VREF to GND)	-0.3 ~ 7	V
V_{OUT}	VOUT Output Voltage (VOUT to GND)	-0.3 ~ $V_{IN}+0.3V$	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air ^(Note 2)	SOP-8	80
		SOP-8P	55
θ_{JC}	Junction-to-Case Thermal Resistance in Free Air ^(Note 3)	20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Note 3: The exposed pad of SOP-8P is soldered directly on the PCB. The case temperature is measured at the center of the exposed pad on the underside of the SOP-8P package.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V _{CNTL}	VCNTL Supply Voltage	3.0 ~ 5.5	V
V _{IN}	VIN Supply Voltage	1.2 ~ 5.5	V
V _{REF}	VREF Input Voltage	0.6 ~ V _{CNTL} - 2.2	V
V _{OUT}	VOUT Output Voltage	V _{REF} ± 0.02	V
I _{OUT}	VOUT Output Current ^(Note 4)	-1.5 ~ +1.5	A
C _{IN}	Capacitance of Input Capacitor	10 ~ 100	μF
	Equivalent Series Resistor (ESR) of Input Capacitor	0 ~ 200	mΩ
C _{OUT}	Capacitance of Output Multi-layer Ceramic Capacitor (MLCC)	8 ~ 47	μF
	Total Output Capacitance ^(Note 5)	10 ~ 330	μF
T _A	Ambient Temperature	-40 ~ 85	°C
T _J	Junction Temperature	-40 ~ 125	°C

Note 4: The symbol “+” means the VO_{UT} sources current to load; the symbol “-” means the VO_{UT} sinks current from load to GND.

Note 5: It’s necessary to use a multi-layer ceramic capacitor 8μF at least as an output capacitor. **Please place the ceramic capacitor near VO_{UT} pin as close as possible.** Besides, the other kinds of capacitors (like Electrolytic, PoSCap, tantalum capacitors) can be used as the output capacitors in parallel.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{CNTL}=5V, V_{IN}=1.8V or 1.5V, V_{REF}=0.5V_{IN}, C_{IN}=10μF, C_{OUT}=10μF (MLCC) and T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

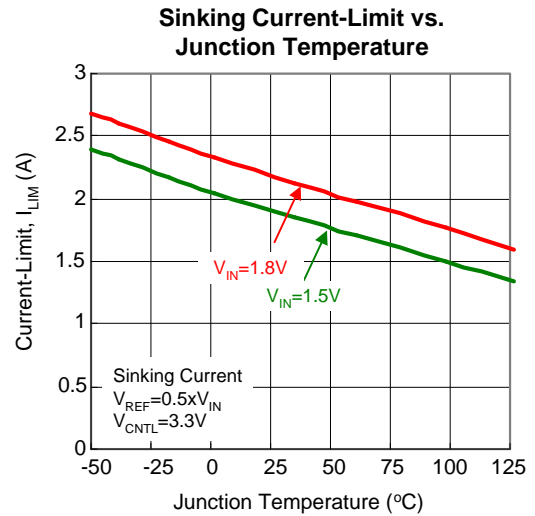
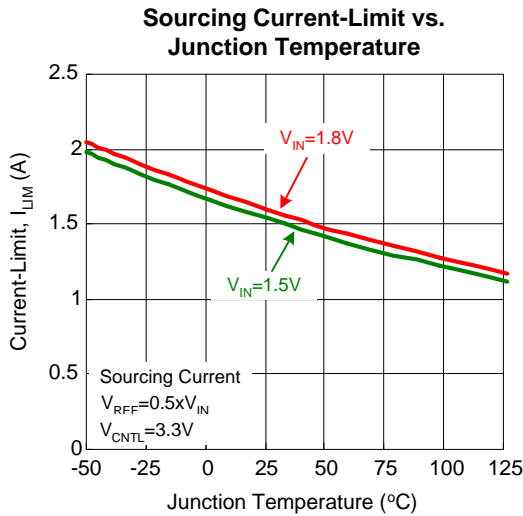
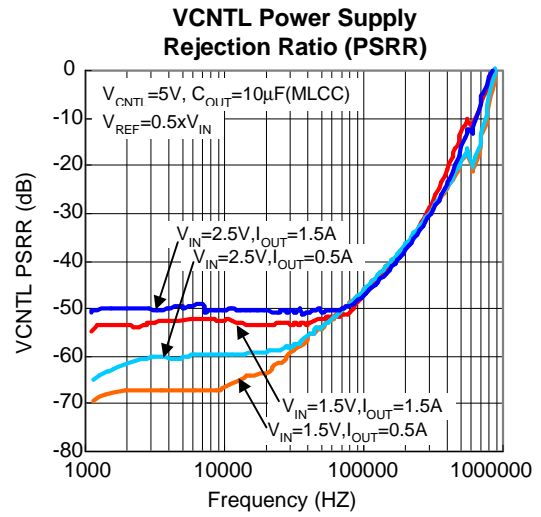
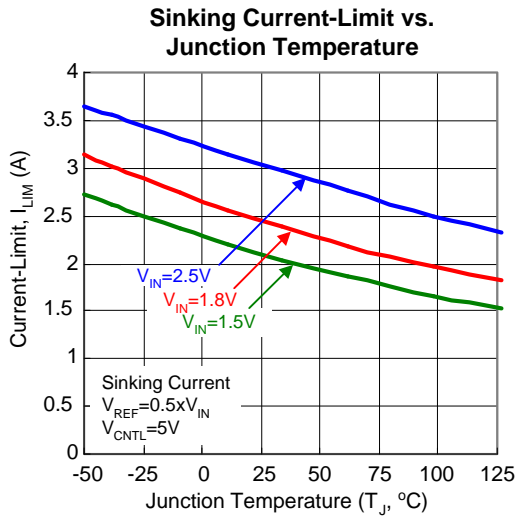
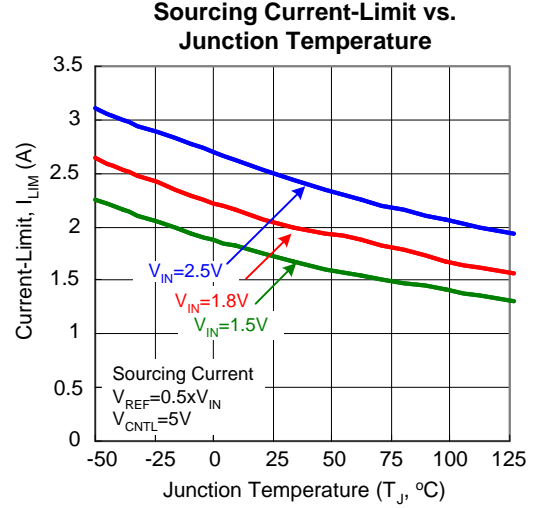
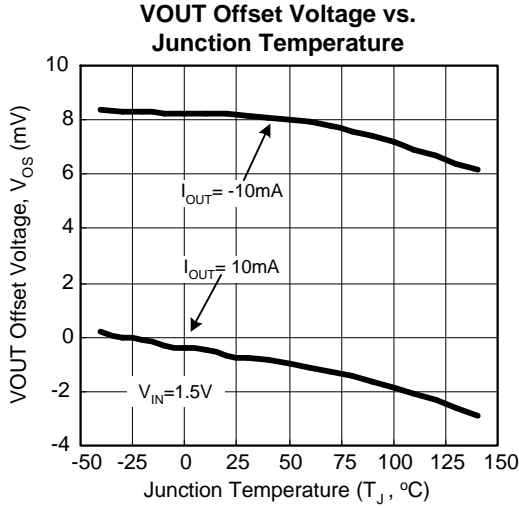
Symbol	Parameter	Test Conditions	APL5336			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I _{CNTL}	VCNTL Supply Current	I _{OUT} = 0A	-	1	2	mA
		V _{REF} =0V (Shutdown)	-	-	5	μA
I _{VIN}	VIN Supply Current at Shutdown	V _{REF} = GND (Shutdown)	-	-	5	μA
POWER-ON-RESET (POR)						
	Rising VCNTL POR Threshold	V _{CNTL} Rising	2.5	2.75	2.9	V
	VCNTL POR Hysteresis		-	0.35	-	V
	Rising VIN POR Threshold	V _{IN} Rising	0.7	0.9	1.05	
	VIN POR Hysteresis		-	0.3	-	V
OUTPUT VOLTAGE						
V _{OUT}	VO _{UT} Output Voltage	I _{OUT} =0A, V _{REF} =0.7V ~ 2.8V	-	V _{REF}	-	V
	System Accuracy	Over temperature and load current ranges	-20	-	20	mV
V _{OS}	VO _{UT} Offset Voltage (V _{OUT} -V _{REF})	I _{OUT} =+10mA	-7	-1	-	mV
		I _{OUT} =-10mA	-	+8	+12	
	Load Regulation	I _{OUT} =+10mA ~ +1.5A	-13	-8	-	mV
		I _{OUT} =-10mA ~ -1.5A	-	+4	+8	

Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over $V_{CNTL}=5V$, $V_{IN}=1.8V$ or $1.5V$, $V_{REF}=0.5V_{IN}$, $C_{IN}=10\mu F$, $C_{OUT}=10\mu F$ (MLCC) and $T_A = -40\sim 85^\circ C$, unless otherwise specified. Typical values are at $T_A=25^\circ C$.

Symbol	Parameter	Test Conditions	APL5336			Unit	
			Min.	Typ.	Max.		
PROTECTIONS							
I_{LIM}	Current-Limit	Sourcing Current ($V_{IN}=1.8V$)	$T_J=25^\circ C$	1.8	2	3	A
			$T_J=125^\circ C$	1.6	-	-	
		Sinking Current ($V_{IN}=1.8V$)	$T_J=25^\circ C$	-2	-2.2	-3	A
			$T_J=125^\circ C$	-1.6	-	-	
		Sourcing Current ($V_{IN}=1.5V$)	$T_J=25^\circ C$	1.6	1.8	2.6	A
			$T_J=125^\circ C$	1.1	-	-	
Sinking Current ($V_{IN}=1.5V$)	$T_J=25^\circ C$	-1.6	-1.8	-2.6	A		
	$T_J=125^\circ C$	-1.1	-	-			
T_{SD}	Thermal Shutdown Temperature	T_J rising	-	150	-	$^\circ C$	
	Thermal Shutdown Hysteresis		-	40	-		
ENABLE AND SOFT-START							
	VREF Enable Voltage Threshold		0.15	0.3	0.4	V	
I_{VREF}	VREF Bias Current		-100	-	+100	nA	
T_{SS}	Soft-Start Interval		0.1	0.2	0.4	ms	

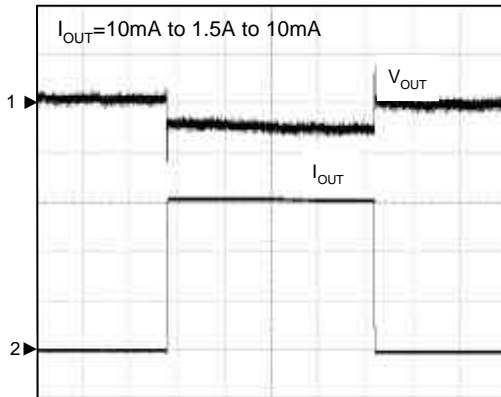
Typical Operating Characteristics



Operating Waveforms

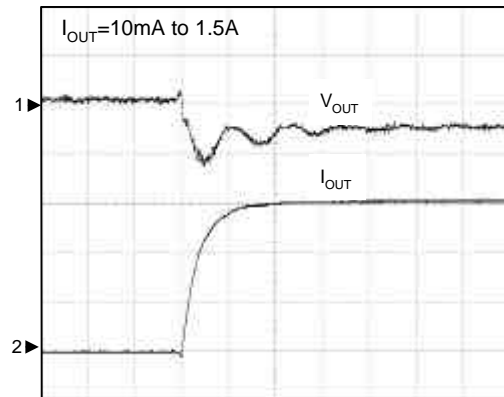
$V_{CNTL} = 5V$, $V_{IN} = 1.8V$ or $1.5V$ or $1.35V$, $V_{REF} = 0.5 \times V_{IN}$, $C_{IN} = C_{OUT} = 10\mu F$ (MLCC)

Load Transient Response ($V_{IN} = 1.8V$)



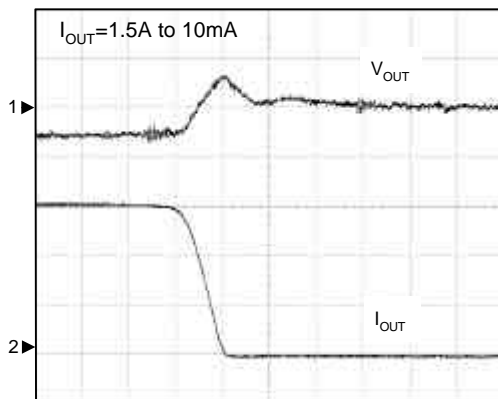
CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 200 μs /Div

Load Transient Response ($V_{IN} = 1.8V$)



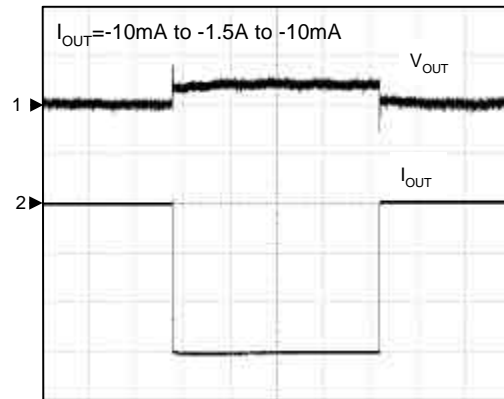
CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μs /Div

Load Transient Response ($V_{IN} = 1.8V$)



CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC

Load Transient Response ($V_{IN} = 1.8V$)

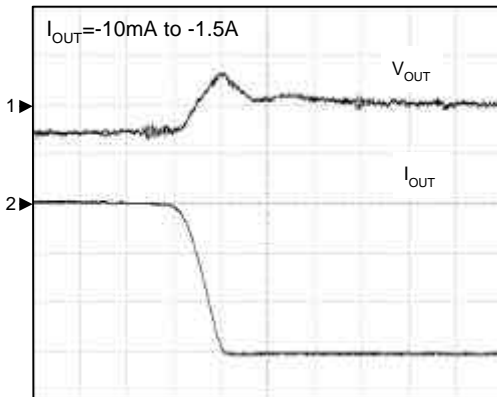


CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 200 μs /Div

Operating Waveforms (Cont.)

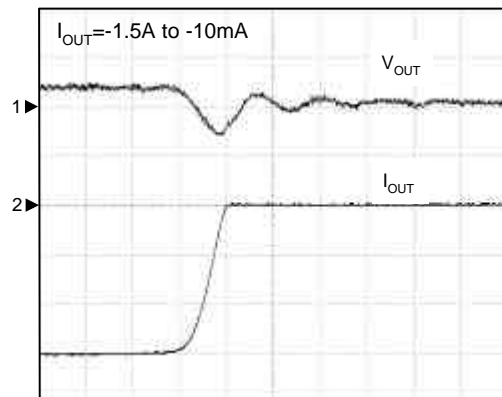
$V_{CNTL} = 5V$, $V_{IN} = 1.8V$ or $1.5V$ or $1.35V$, $V_{REF} = 0.5 \times V_{IN}$, $C_{IN} = C_{OUT} = 10\mu F$ (MLCC)

Load Transient Response ($V_{IN} = 1.8V$)



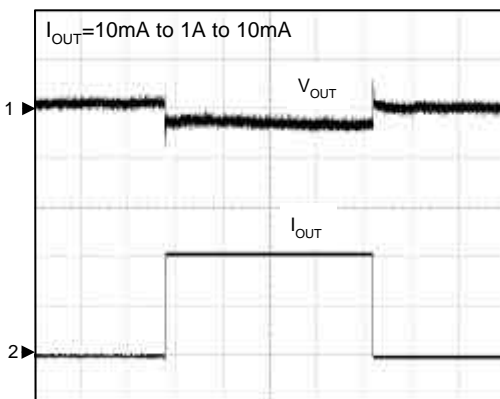
CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μ s/Div

Load Transient Response ($V_{IN} = 1.8V$)



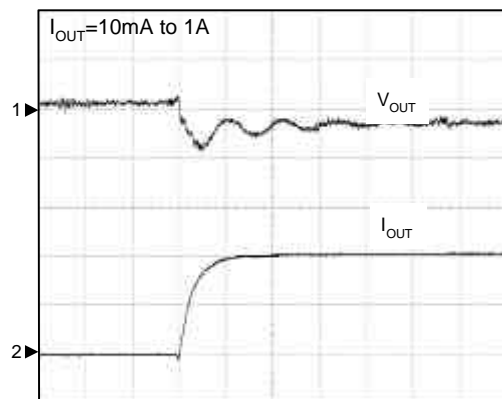
CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μ s/Div

Load Transient Response ($V_{IN} = 1.5V$)



CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 200 μ s/Div

Load Transient Response ($V_{IN} = 1.5V$)

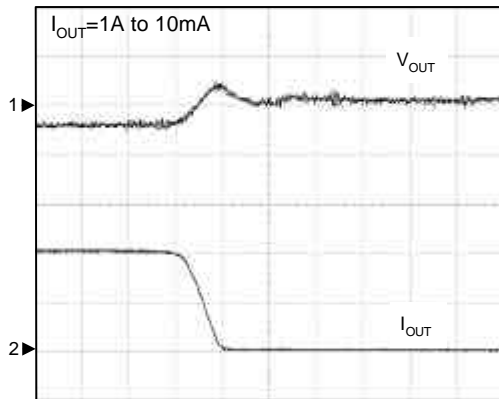


CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μ s/Div

Operating Waveforms (Cont.)

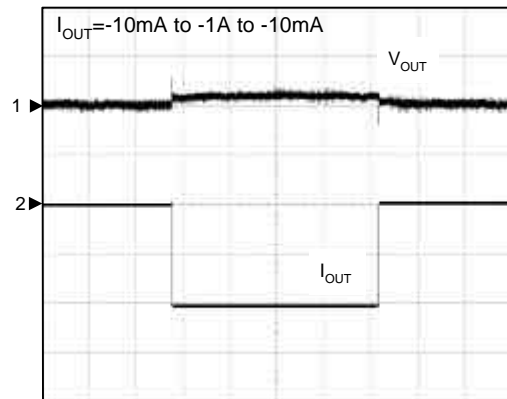
$V_{CNTL} = 5V$, $V_{IN} = 1.8V$ or $1.5V$ or $1.35V$, $V_{REF} = 0.5 \times V_{IN}$, $C_{IN} = C_{OUT} = 10\mu F$ (MLCC)

Load Transient Response ($V_{IN} = 1.5V$)



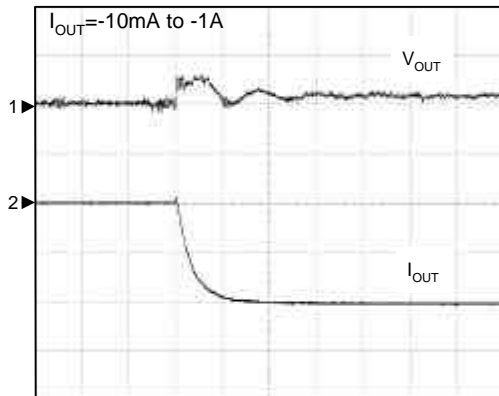
CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μ s/Div

Load Transient Response ($V_{IN} = 1.5V$)



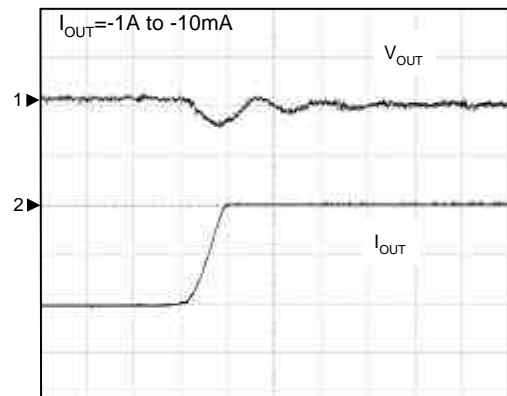
CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 200 μ s/Div

Load Transient Response ($V_{IN} = 1.5V$)



CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μ s/Div

Load Transient Response ($V_{IN} = 1.5V$)

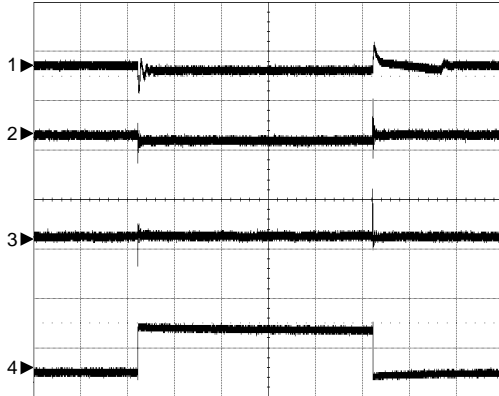


CH1: V_{OUT} , 20mV/Div, AC
 CH2: I_{OUT} , 0.5A/Div, DC
 TIME: 1 μ s/Div

Operating Waveforms (Cont.)

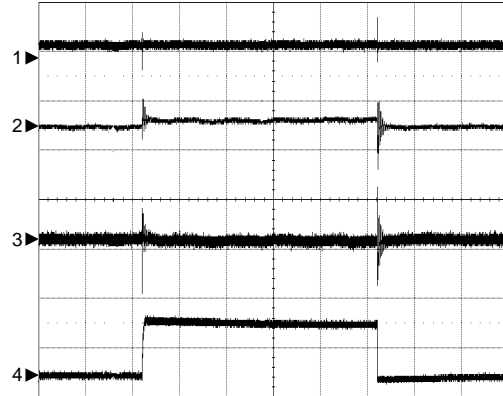
$V_{CNTL} = 5V$, $V_{IN} = 1.8V$ or $1.5V$ or $1.35V$, $V_{REF} = 0.5 \times V_{IN}$, $C_{IN} = C_{OUT} = 10\mu F$ (MLCC)

VREF=0.675V Load Transient (Source)



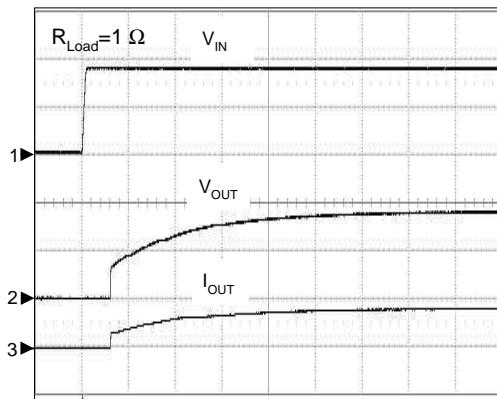
$V_{CNTL} = 3.3V$, $V_{REF} = 0.675V$, $V_{IN} = 1.35V$
 CH1: V_{IN} , 100mV/Div, DC, Offset=1.35V
 CH2: V_{OUT} , 50mV/Div, DC, Offset=0.675V
 CH3: V_{REF} , 50mV/Div, DC, Offset=0.675V
 CH4: I_{OUT} , 1A/Div, DC
 TIME: 0.2mS/Div

VREF=0.675V Load Transient (Sink)



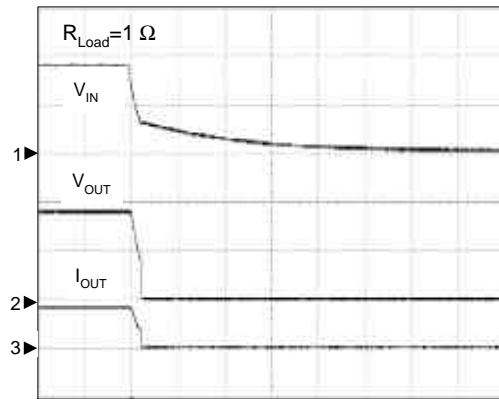
$V_{CNTL} = 3.3V$, $V_{REF} = 0.675V$, $V_{IN} = 1.35V$
 CH1: V_{IN} , 50mV/Div, DC, Offset=1.35V
 CH2: V_{OUT} , 20mV/Div, DC, Offset=0.675V
 CH3: V_{REF} , 20mV/Div, DC, Offset=0.675V
 CH4: I_{OUT} , 1A/Div, DC
 TIME: 0.2mS/Div

Power ON Test ($V_{IN} = 1.8V$)



CH1: V_{IN} , 1V/Div, DC
 CH2: V_{OUT} , 500mV/Div, DC
 CH3: I_{OUT} , 1A/Div, DC
 TIME: 50ms/Div

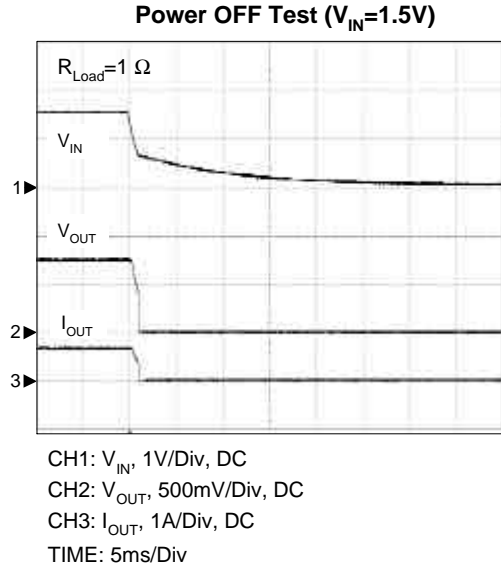
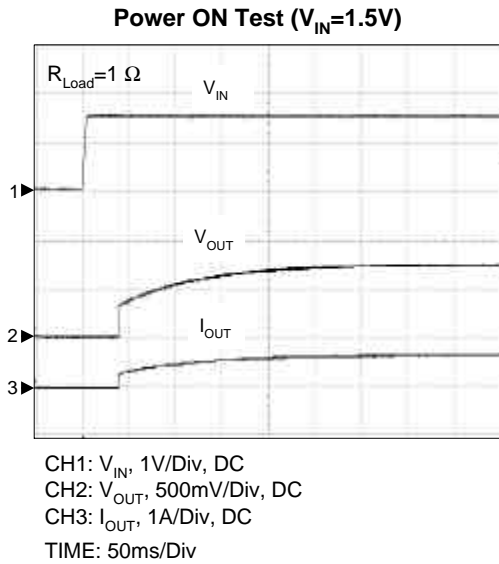
Power OFF Test ($V_{IN} = 1.8V$)



CH1: V_{IN} , 1V/Div, DC
 CH2: V_{OUT} , 500mV/Div, DC
 CH3: I_{OUT} , 1A/Div, DC
 TIME: 5ms/Div

Operating Waveforms (Cont.)

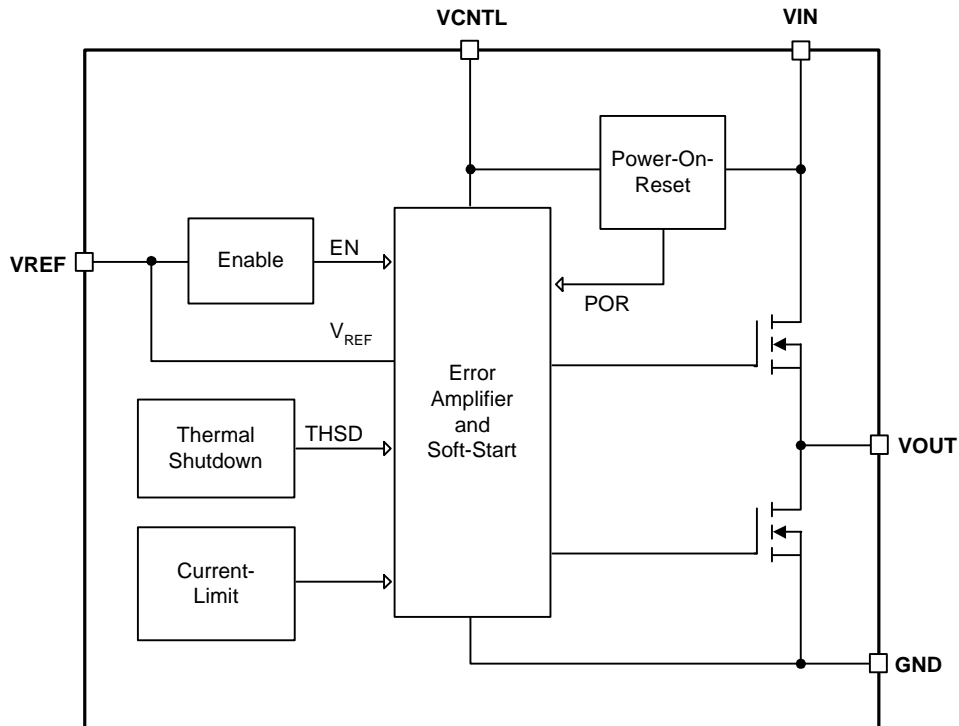
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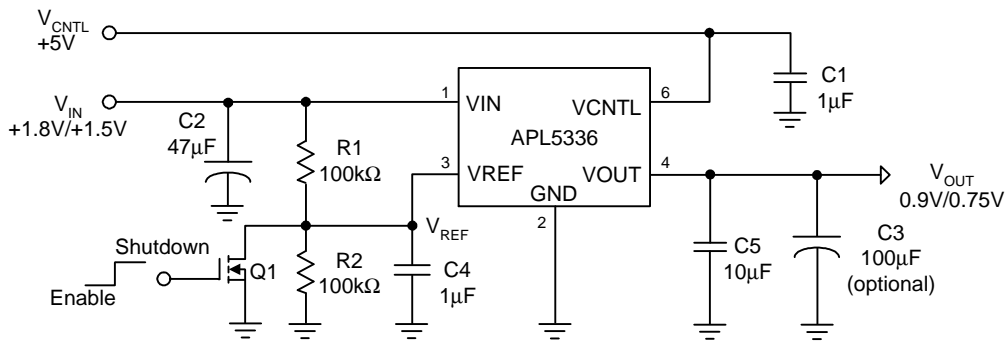
Pin Description

PIN			FUNCTION
NO.		NAME	
SOP-8	SOP-8P		
1	1	VIN	Main Power Input Pin. Connect this pin to a voltage source and an input capacitor. The APL5336 sources current to VOUT pin by controlling the upper pass MOSFET, providing a current path from VIN to VOUT.
2	2	GND	Power and Signal Ground. Connect this pin to system ground plane with shortest traces. The APL5336 sinks current from VOUT pin by controlling the lower pass MOSFET, providing a current path from VOUT to GND. This pin is also the ground path for internal control circuitry.
3	3	VREF	Reference Voltage Input and Active-high Enable Control Pin. Apply a voltage to this pin as a reference voltage for the APL5336. Connect this pin to a resistor divider, between VIN and GND, and a capacitor for filtering noise purpose. Applying and holding the voltage below the enable voltage threshold on this pin by an open-drain transistor shuts down the output. During shutdown, the VOUT pin has high input impedance.
4	4	VOUT	Output Pin of The Regulator. Connect this pin to load and output capacitors (>8μF MLCC is necessary) required for stability and improving transient response. The output voltage is regulated to track the reference voltage and capable of sourcing or sinking current up to 1.5A.
-	5, 7, 8	NC	No Internal Connection.
5, 6, 7, 8	6	VCNTL	Power Input Pin for Internal Control Circuitry. Connect this pin to a voltage source, providing a bias for the internal control circuitry. A decoupling capacitor is connected near this pin.
-	Exposed Pad	GND	Chip Substrate Connection of The Chip. Connect this pad to system ground plane for good thermal conductivity.

Block Diagram



Typical Application Circuit



The ceramic capacitor C5 (at least 8µF) is necessary for output stability.

Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on.

Output Voltage Regulation

The output voltage on VOUT pin is regulated to track the reference voltage applied on VREF pin. Two internal N-channel power MOSFETs controlled by high bandwidth error amplifiers regulate the output voltage by sourcing current from VIN pin or sinking current to GND pin. An internal output voltage sense pad is bonded to the VOUT pin with a bonding wire for perfect load regulation.

For preventing the two power MOSFETs from shoot-through, a small voltage offset between the positive inputs of the two error amplifiers is designed. It results in higher output voltage while the regulator sinks light or heavy load current.

The APL5336 provides very fast load transient response at small output capacitance to save total cost.

Current-Limit

The APL5336 monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short-circuit (shorted from VOUT to GND or VIN) conditions.

Enable

The VREF pin is a multi-function input pin which is the reference voltage input pin and the enable control input pin. Applying and holding the voltage (V_{REF}) on VREF below 0.3V (typical) shuts down the output of the regulator. In the typical application, an NPN transistor or N-channel MOSFET is used to pull down the V_{REF} while applying a “high” signal to turn on the transistor. When shutdown function is active, both of the internal power MOSFETs are turned off and the impedance of the VOUT pin is larger than 10M Ω .

Internal and External Soft-Start

The APL5336 is designed with an internal soft-start function to control the rise rate of the output voltage to prevent inrush current during start-up.

When release the pull-low transistor connected with VREF pin, the current via the resistor divider charges the external soft-start capacitor (C4) and the V_{REF} starts to rise up. The IC starts a soft-start process when the V_{REF} reaches the enable voltage threshold. The output voltage is regulated to follow the lower voltage, which is either the internal soft-start voltage ramp or the VREF voltage, to rise up. The external soft-start interval is programmable by the resistor-divider and the soft-start capacitor (C4).

Thermal Shutdown

The thermal shutdown circuit limits the junction temperature of the APL5336. When the junction temperature exceeds 150°C, a thermal sensor turns off the both pass transistors, allowing the device to cool down. The thermal sensor allows the regulator to regulate again after the junction temperature cools by 40°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal limit is designed with a 40°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the APL5336.

Application Information

Power Sequencing

The input sequence of powers applied for VIN and VCNTL is not necessary to be concerned.

Reference Voltage

A reference voltage is applied at the VREF pin by a resistor divider between VIN and GND pins. An external bypass capacitor is also connected to VREF. The capacitor and the resistor divider form a low-pass filter to reduce the inherent reference noise from VIN. The capacitor is a 0.1μF or greater ceramic capacitor and connected as close to VREF as possible. More capacitance and large resistor divider will increase the soft-start interval. Do not place any additional loading on this reference input pin.

Input Capacitor

The APL5336 requires proper input capacitors to supply current surge during stepping load transients to prevent the input rail from dropping. Because the parasitic inductors from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the input current, more parasitic inductance needs more input capacitance. For the APL5336, the total capacitance of input capacitors value including MLCC and aluminum electrolytic capacitors should be larger than 10μF.

For VCNTL pin, a capacitor of 0.47μF (MLCC) or above is recommended for noise decoupling.

Output Capacitor

The APL5336 needs a proper output capacitor to maintain circuit stability and improve transient response. In order to insure the circuit stability, a 10μF X5R or X7R MLCC output capacitor is sufficient at all operating temperatures and it must be placed near the VOUT. The maximum distance from output capacitor to VOUT must within 10mm. Total output capacitors value including MLCC and aluminum electrolytic capacitors should be larger than 10μF.

Table 1: Output Capacitor Guide

Vendor	Description
Murata	10μF, 6.3V, X7R, 0805, GRM21BR70J106K
	10μF, 6.3V, X5R, 0805, GRM21BR60J106K

Murata website: www.murata.com

Table 1 provides the suitable output capacitors for APL5336.

Operation Region and Power Dissipation

The APL5336 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D \leq \frac{(T_J - T_A)}{\theta_{JA}}$$

Where $(T_J - T_A)$ is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the $T_A = 25^\circ\text{C}$ and maximum $T_J = 150^\circ\text{C}$ (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(\max)} = \frac{(150 - 25)}{80} = 1.56(\text{W})$$

For normal operation, do not exceed the maximum junction temperature of $T_J = 125^\circ\text{C}$. The calculated power dissipation should less than:

$$P_D = \frac{(125 - 25)}{80} = 1.25(\text{W})$$

PCB Layout Consideration

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Please place the output capacitors close to the VOUT, a MLCC capacitor larger than 8μF must be placed near the VOUT. The distance from VOUT to output MLCC must be less than 10mm.
3. To place APL5336 and output capacitors near the load is good for load transient response.
4. Large current paths, the bold lines in Figure 1, must have wide tracks.
5. For SOP-8P package, please solder the thermal pad to the APL5336 to top-layer ground plane. Numerous vias 0.254mm in diameter should be used to connect both top-layer and internal ground planes. The ground planes and PCB form a heat sink to channel major power dissipation of the APL5336 into ambient air.

Large ground plane is good for heatsinking. Optimum performance can only be achieved when the device is mounted on a PC board according to the board layout diagrams which are shown as Figure 2.

Application Information (Cont.)

PCB Layout Consideration (Cont.)

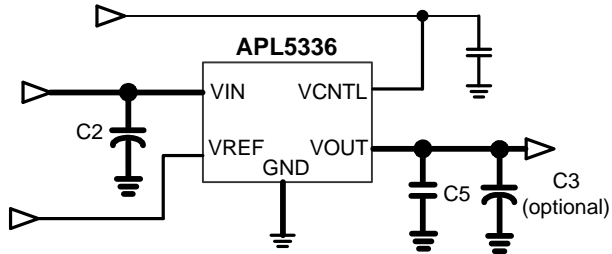
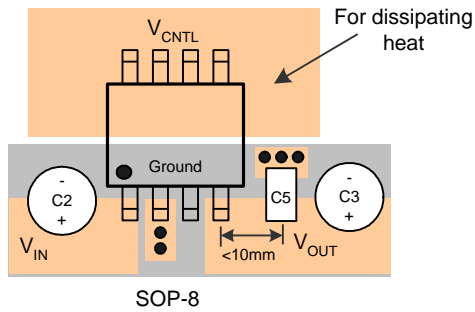
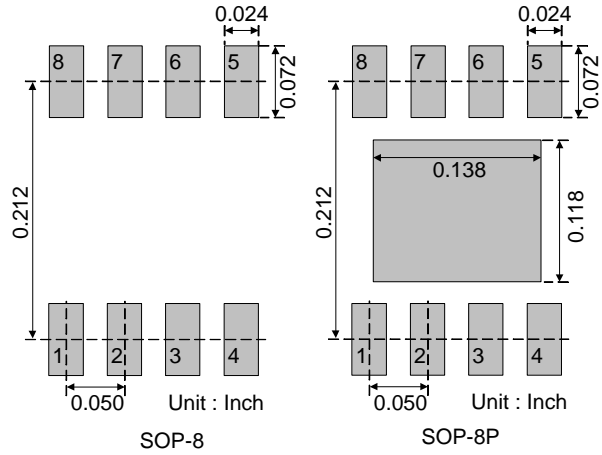
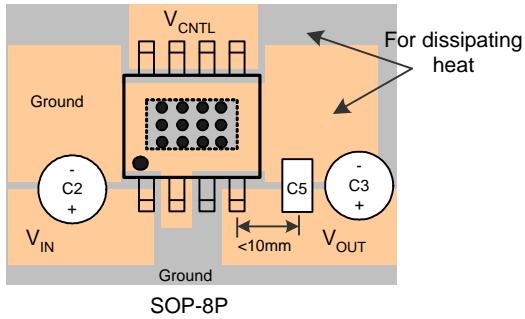


Figure 1.

Recommended Minimum Footprint



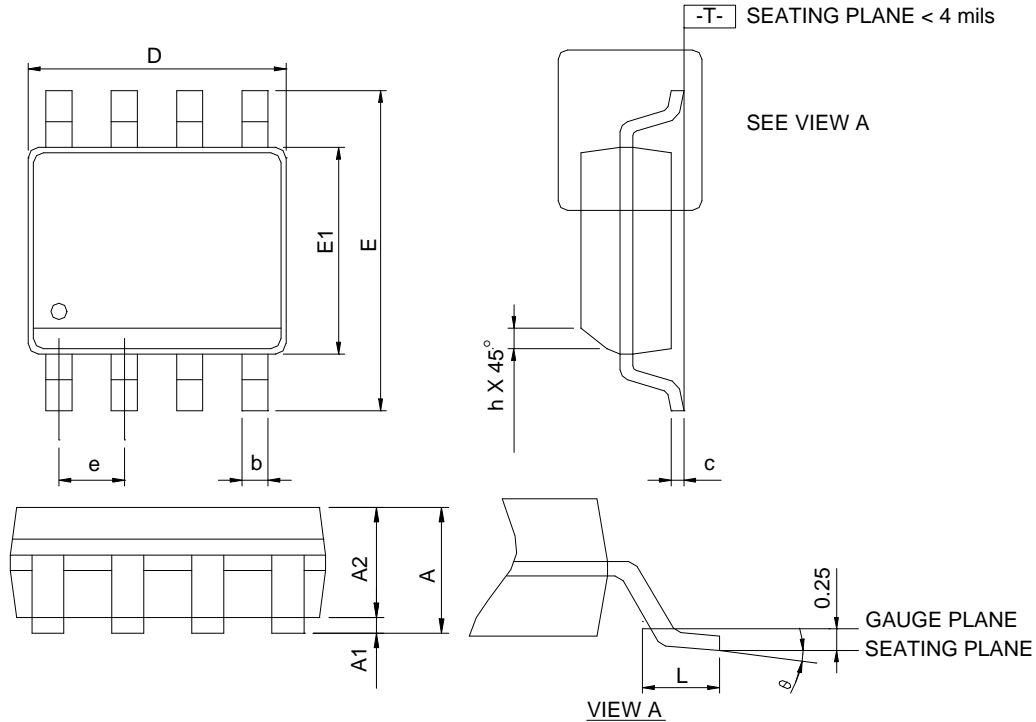
SOP-8



SOP-8P

Package Information

SOP-8

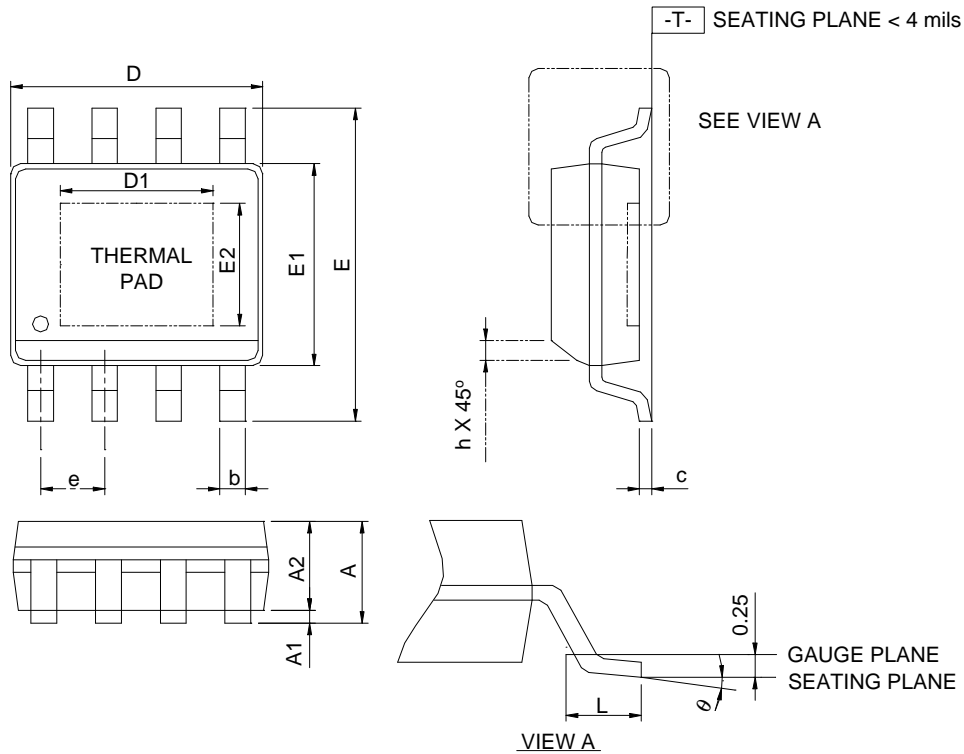


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

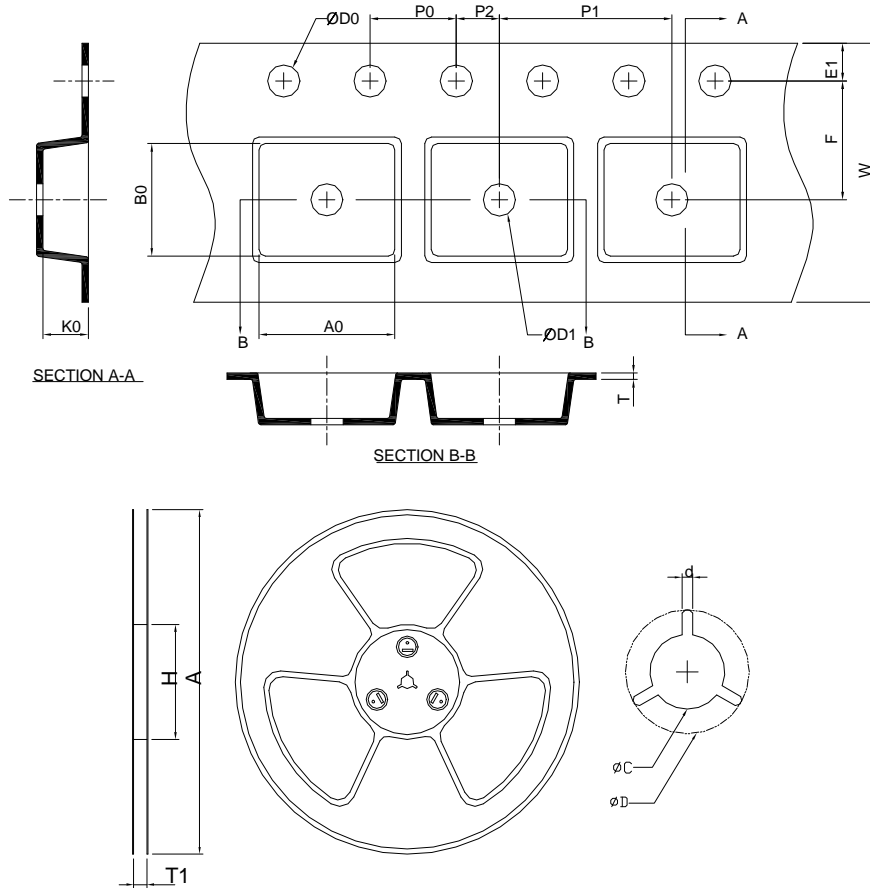
SOP-8P



DIMENSIONS	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

- Note : 1. Followed from JEDEC MS-012 BA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8(P)	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20

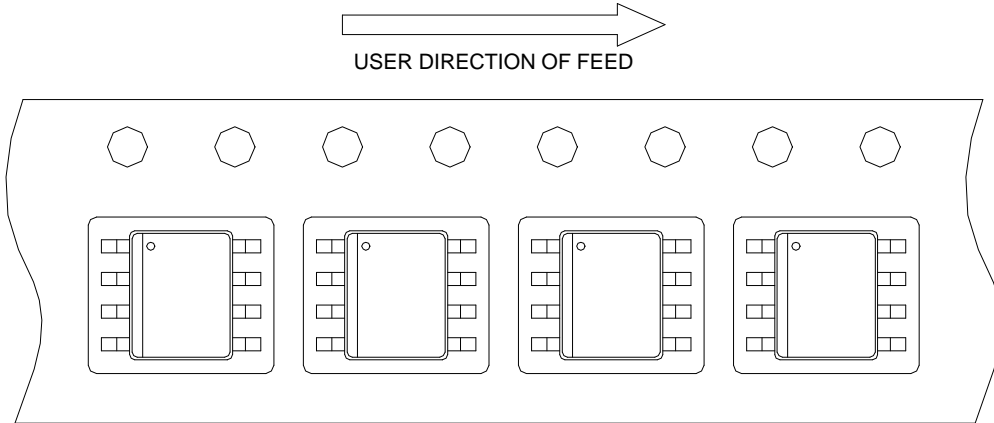
(mm)

Devices Per Unit

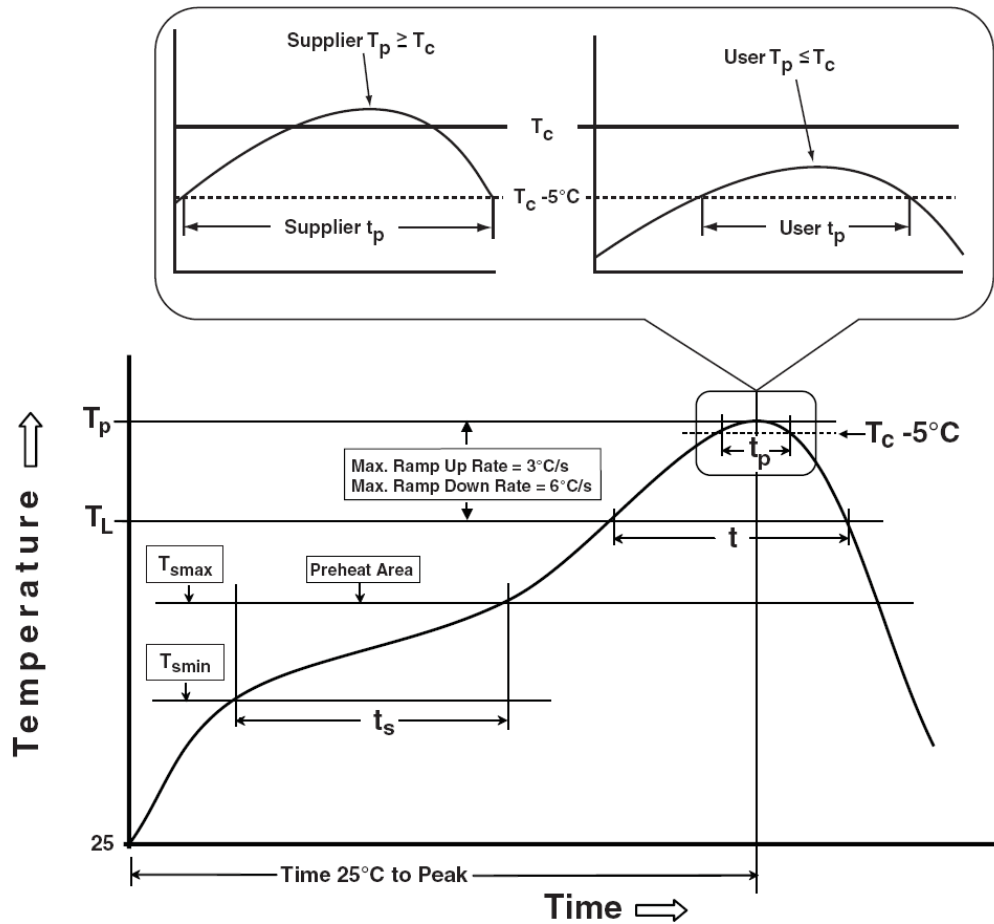
Package Type	Unit	Quantity
SOP-8(P)	Tape & Reel	2500

Taping Direction Information

SOP-8(P)



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 _{tr} 100mA

Customer Service

Anpec Electronics Corp.

Head Office :

No.6, Dusing 1st Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,

Sindian City, Taipei County 23146, Taiwan

Tel : 886-2-2910-3838

Fax : 886-2-2917-3838