APE5030A

16 Channel LED Controller for LCD Backlight

Features

- **Wide range input is 9V to 24V**
- **High Accurate LED Current 1%Typ.(ILED=120mA)**
- **16 Channel flexible PFM genrators and independent for 14 Bits PFM brigntness**
- **Synchronization with TV Frame - VSYNC / HSYNC / Digital PLL Integrated**
- **Digital Configurable DC/DCFeedback**
- **Protection For Safety Features**
  - **LED Short Detection**
  - **LED Open Detection**
  - **Temperature Shutdown detection**
  - **UVLO**
- **PFM Dimming Via SPI Interface**
- **Adaptive Control Mode For High Efficiency**
- **Available In QFN 7x7-48 Package**
- **One global high accurate 10 bit DAC which sets the LED current.**

Applications

- **Televisions**
- **Monitors**

General Description

The APE5030A are integrates Mosfet and 16 channel LED controller for LCD backlight. It's high accurate LED current 1% (120mA LED current) and wide input voltage range.
The APE5030A has 16 Channel flexible PFM genrators and independent 14 bits PFM brigntness were control LED current for every channel. in addition; It's has one global high accruate 10 bit DAC which sets the LED current. It's synchronization with TV Frame including VSYNC/HSYNC and Digital PLL method.
The APE5030A has two pin can be digital configurable DC/DC feedback, that's for control DC/DC architecture. As the same time; the device using programmable via SPI interface.
The version APE5030A is factory pre-programmed to Direct_PWM is "1" but it can still be configured via the SPI interface. (e.g. switch to internal PFM generation) In this mode APE5030A has the following default configuration after power on:
• All current outputs are ON
• All feedback controls are enabled and connected to FB1
• OPEN LED detection is enabled
• OPEN LED detection auto turn off is enabled
• OPEN LED detection retrial function is enabled
• SHORT LED detection (SHORT-COMP) is enabled
• SHORT LED detection auto turn off is enabled
• Undervoltage lockout and over temperature detection are enabled
The APE5030A own adaptive control mode for high efficiency. it's build-in protection for safety, include LED short, LED Open, temperature shutdown protection and UVLO. The APE5030A has adaptive control mode method for high efficiency and increase power loss cause to temperature. The APE5030A is available in QFN 7x7-48 packages.

Ordering and Marking Information

APE5030A □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

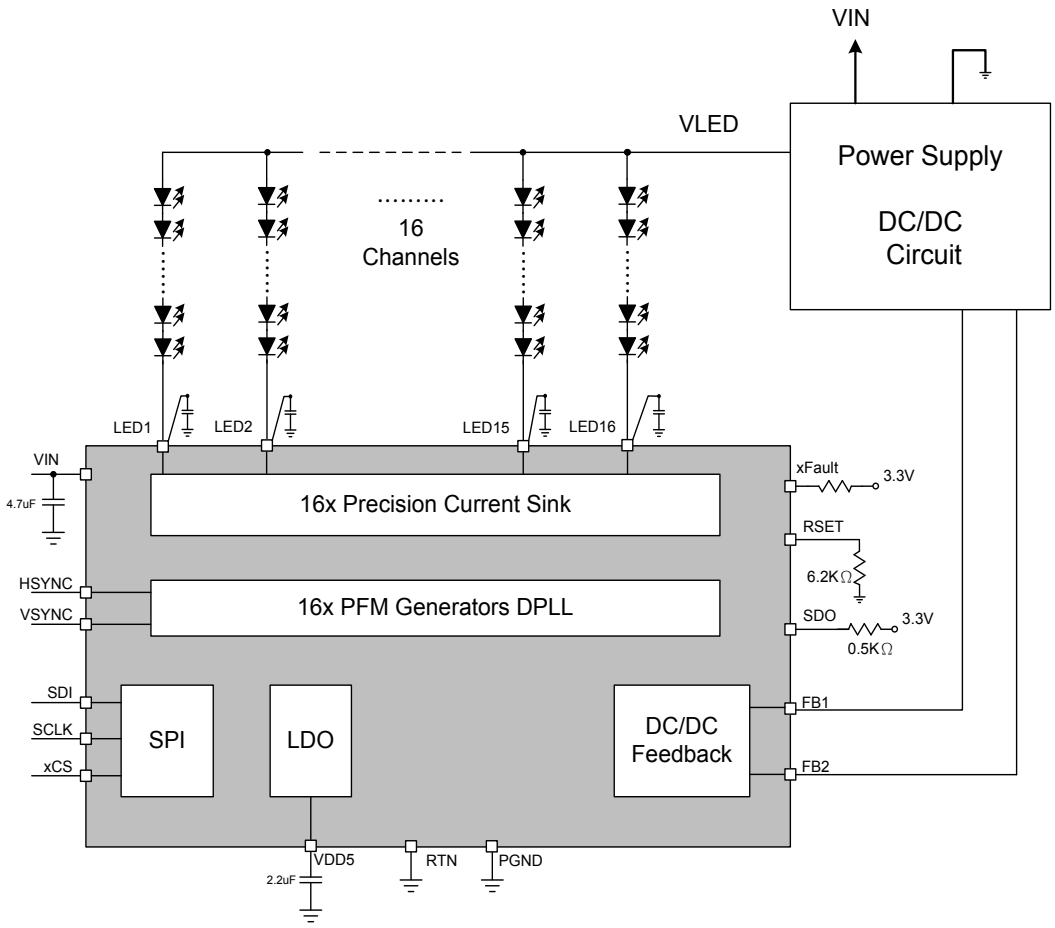
Package Code
QA: QFN7x7-48
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Lead Free Code
L : Lead Free Device G : Halogen and Lead Free Device

APE5030A QA :

XXXXX - Date Code

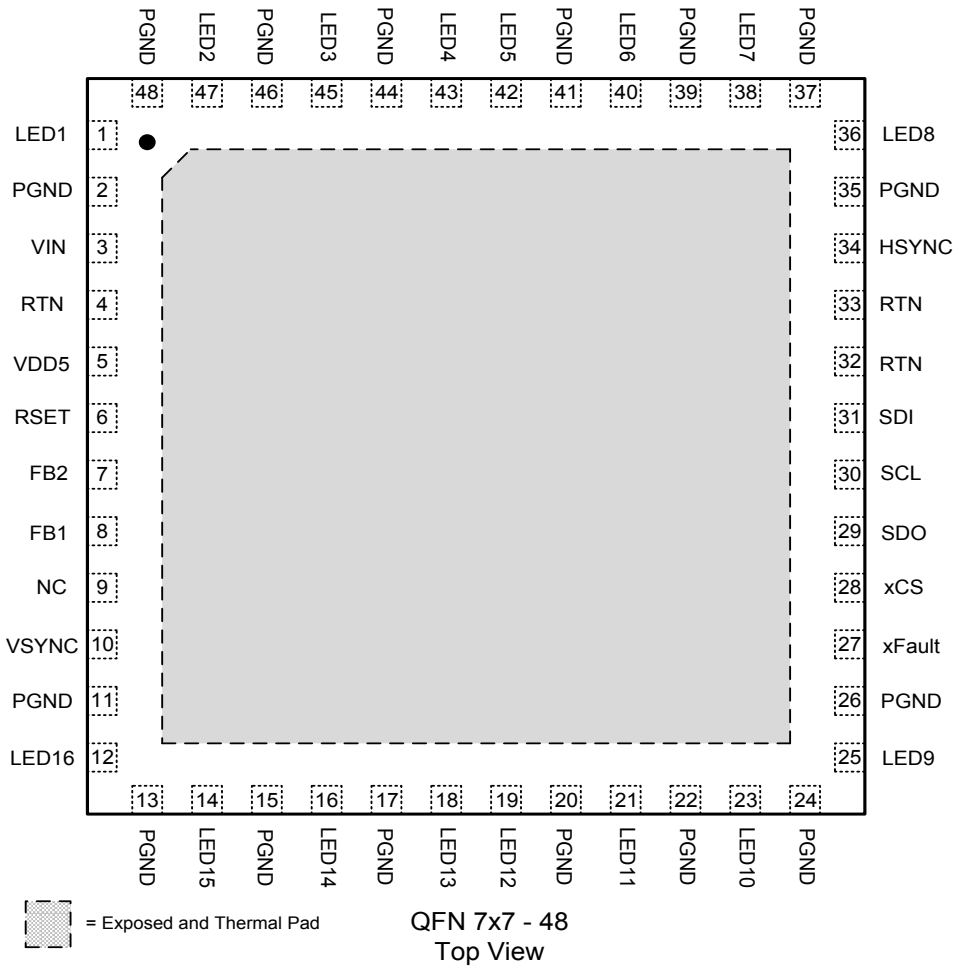
Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Simplified Application Circuit



Note:When LED1 to 16 of APE5030A pin-out location to external LED string cathode location has execcd 1uH wire inducutance, suggestion add the MLCC capcitors for holdout interference.

Pin Configurations



QFN 7x7 - 48
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to PGND)	-0.3 ~ 26	V
V_{ANALOG}	LED1~LED16 to PGND	-0.3 ~ 60	V
	VSYNC, HSYNC, FB1, FB2 and RSET to PGND	-0.3 ~ 7	V
$V_{DIGITAL}$	VDD5, SDI, SDO, SCL, xCS and xFault to RTN	-0.3 ~ 7	V
V_{GND}	RTN to PGND	-0.3 ~ +0.3	V
T_J	Junction Temperature	180	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	35	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{IN}	Input Supply Voltage	9 ~ 24	V
V_{LEDn}	LED String Voltage	~60	V
I_{LED}	LED Current	20 ~ 250	mA
C_{IN}	Input Voltage Capacitor	4.7~	uF
C_{VDD5}	VDD5 Output Capacitor	2.2~	uF
R_{SET}	External Setting LED Current Resistor	6.2±1%	KΩ
T_A	Ambient Temperature	-20 ~ 85	°C
T_J	Junction Temperature	-20 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APE5030A			
			Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage Range		9	-	24	V
V_{LDO}	LDO Voltage Regulation Output	I_{LOAD}=20mA	4.5	5	5.5	V
V_{IN-POR}	VIN Power On Reset Level	VIN Rising	7.5	8	8.5	V
V_{IN_UVLO}		VIN Falling	-	1	-	V
		Turn Off ILED Current	-	7.6	-	V
	Power On Delay Time	VIN POR to Command Time	-	10	-	ms
I_Q	Quiescent Current	VIN=9V, Default Setting (Standby mode)	-	-	20	mA
		VIN=9V, VDAC_Reg_Code[9:0]=4 Clocksrc0 0x13 bit[6] ="0" and clocksrc0 0x13 bit [5]="1"	-	-	3	mA
	Shutdown Current	VIN=9V, 0x59 bit [0]=0 to 1	-	-	1	mA
$I_{LED\_250\_120}$	Current Accuracy	ILED=119.96mA, REG_ Code[9:0]=476, 25 °C (Note:It's not include RSET)	-1	-	1	%
$I_{LED\_250\_20}$	Current Accuracy	ILED=19.91mA, REG_Code[9:0]=79, 25 °C (Note:It's not include RSET)	-2	-	2	%
$I_{LED\_250\_250}$	Current Accuracy	ILED=250mA, REG_ Code[9:0]=992,25 °C (Note:It's not include RSET)	-2	-	2	%

Electrical Characteristics (Cont.)

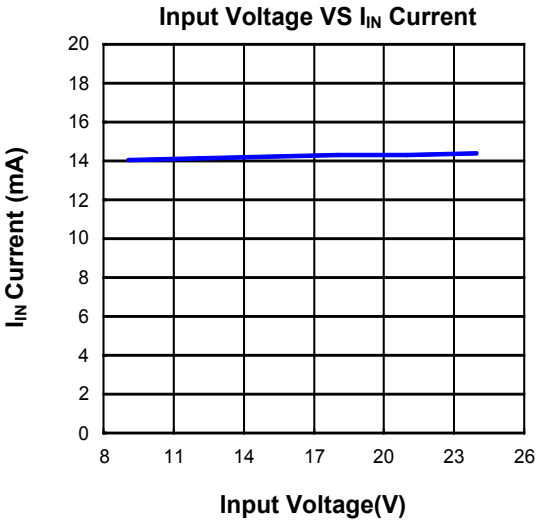
Unless otherwise specified, these specifications apply over V_{IN}=12V, and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

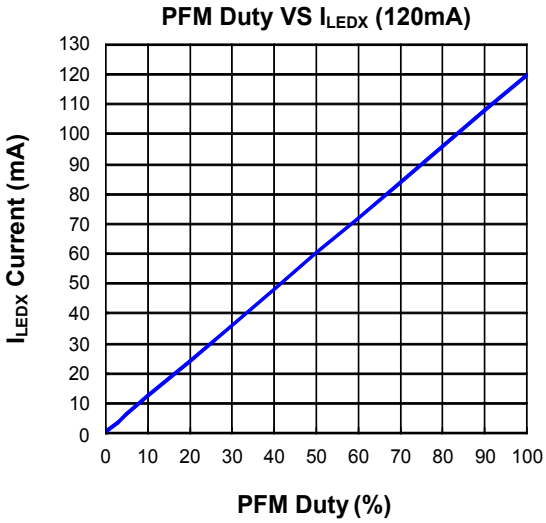
Symbol	Parameter	Test Condition	APE5030A			
			Min.	Typ.	Max.	Unit
$I_{LED\_800\_ALL}$	LED Current Accuracy to All Temperature	I_{LED}=119.96mA, REG_Code[9:0]=476, -25 ~ 85 °C	-2	-	2	%
		I_{LED}=250mA, REG_Code[9:0]=992, -25 ~ 85 °C	-2.5	-	2.5	%
		I_{LED}=19.91mA, REG_Code[9:0]=79, -25 ~ 85 °C	-2.5	-	2.5	%
I_{LED_CH}	Channel to channel current matching	I_{LED}=119.96mA,25 °C (Note:It's not include RSET)	-2	-	2	%
I_{FB_MAX}	Feedback Current Maximum	V_{FB}_X > 0.25V	251	255	259	uA
FB_{IDAC_LSB}	FB_DAC_LSB		-	1	-	uA
T_{OTP}	Over-temperature	Temperature rising	145	160	175	°C
T_{OTP_HYS}	Temperature hysteresis		-	20	-	°C
T_{SHORT_MIN}	Minimum PFM on time to detect shorted LEDs		-	10	-	us
F_{OSC}	Internal Clock for PFM		7.2	8	8.8	MHz
F_{HSYNC}	HSYNC Frequency		100	-	20000	KHz
F_{VSYNC}	VSYNC Frequency		60	-	40000	Hz
V_{VSYNC}	VSYNC Duration		5	-	-	us
V_{IH}	High Level Input Voltage	Input PIN (VSYNC, HSYNC, xCS, SCL,SDI	1.7	-	V_{DD5}+ 0.3	V
V_{IL}	Low Level Input Voltage	Input PIN (VSYNC, HSYNC, xCS, SCL,SDI	-0.3	-	1	V
V_{OH}	High Level Output Voltage	Output PIN, (xFAULT) I=2mA	VDD5-0.3	-	-	V
V_{OL}	Low Level Output Voltage	Output PIN, (xFAULT) I=2mA	-	-	0.3	V
V_{OL_PD}	Low Level Output Voltage Open Drain Outputs	I=2mA	-	-	0.3	V
R_{PU}	Input Resistance Pull-up	VIN=12V, xCS=GND	-	300	-	KΩ
R_{PD}	Input Resistance Pull-down	VIN=12V,VSYNC, HSYNC, SCL, SDI=5V	-	300	-	KΩ
I_{LEK}	Leakage Current	VIN=12V, For xFault, FB1, FB2	-	-	1	μA

Pin Description

PIN		FUNCTION
NO.	NAME	
1	LED1	LED Cathode Connection For LED String1.
2, 11, 13, 15, 17, 20, 22, 24, 26, 35, 37, 39, 41, 44, 46, 48	PGND	Power Ground For LED Current Return Path.
3	VIN	Input Supply Voltage.
4,32	RTN	Analog Ground.
5	VDD5	Internal 5V LDO For Analog and Digital Circuit.
6	RSET	External Setting Iset Current Resistor, RSET to GND connection 6.2K (±1%)
7	FB2	DC/DC Power Supply Feedback Output2
8	FB1	DC/DC Power Supply Feedback Output1
9	NC	No Connection.
10	VSYNC	Vertical sync frequency. PFM Generator Reset
12	LED16	LED Cathode Connection For LED String16.
14	LED15	LED Cathode Connection For LED String15.
16	LED14	LED Cathode Connection For LED String14.
18	LED13	LED Cathode Connection For LED String13.
19	LED12	LED Cathode Connection For LED String12.
21	LED11	LED Cathode Connection For LED String11.
23	LED10	LED Cathode Connection For LED String10.
25	LED9	LED Cathode Connection For LED String9.
27	xFault	Open Drain Fault Output, Connect Pull-up to VDD5
28	xCS	SPI Interface Chip Select.
29	SDO	SPI Interface Data Output. Tristate Output
30	SCL	SPI Interface Clock
31	SDI	SPI Interface Data Input
33	RTN	Digital and I/O Ground.
34	HSYNC	Clock Input For PFM Generators
36	LED8	LED Cathode Connection For LED String8.
38	LED7	LED Cathode Connection For LED String7.
40	LED6	LED Cathode Connection For LED String6.
42	LED5	LED Cathode Connection For LED String5.
43	LED4	LED Cathode Connection For LED String4.
45	LED3	LED Cathode Connection For LED String3.
47	LED2	LED Cathode Connection For LED String2.

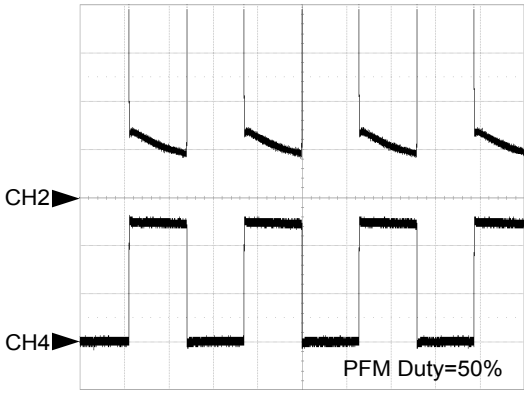
Typical Operating Characteristics





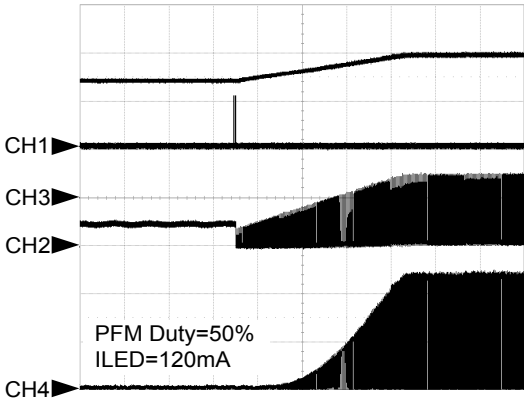
OperatingWaveforms

Normal Operation
(ILED=250mA)



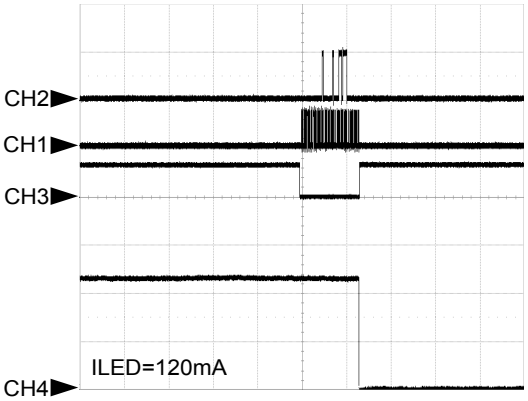
CH1:-
CH2:LEDx V_{Drain}-500mV/div
CH3:-
CH4:I_{LEDx}-100mA/div
Time:200us/div

Start up – Current on enable



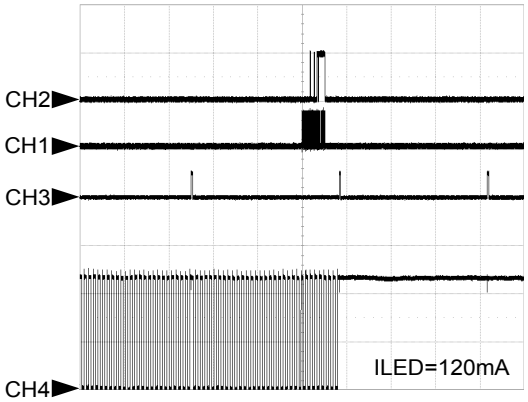
CH1:V_{SDI}-5V/div
CH2:$V_{LED\ Drain}$-5V/div
CH3:V_{OUT}-10V/div
CH4:I_{LEDx}-50mA/div
Time:20ms/div

Update Mode (xCS)
PFM duty 100% to 0%



CH1:V_{SDI}-5V/div
CH2:V_{SCL}-5V/div
CH3:V_{xCS}-5V/div
CH4:I_{LEDx}-50mA/div
Time:2ms/div

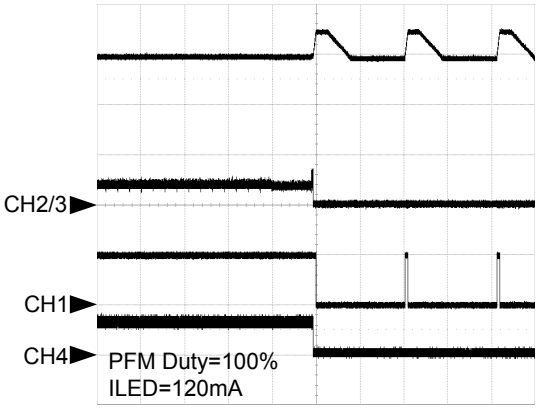
Update Mode (Vsync)
PFM duty 50% to 100%



CH1:V_{SDI}-5V/div
CH2:V_{SCL}-5V/div
CH3:V_{SYNC}-10V/div
CH4:I_{LEDx}-50mA/div
Time:5s/div

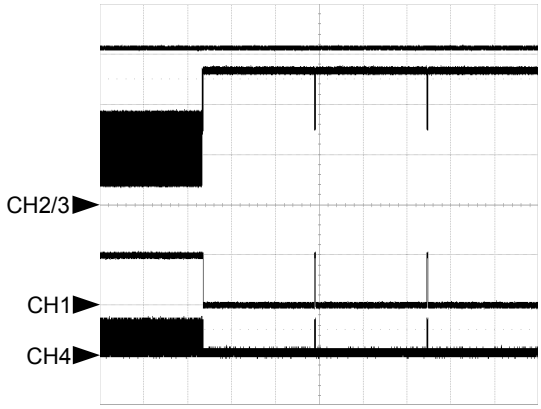
OperatingWaveforms (Cont.)

Open LED - Retrial



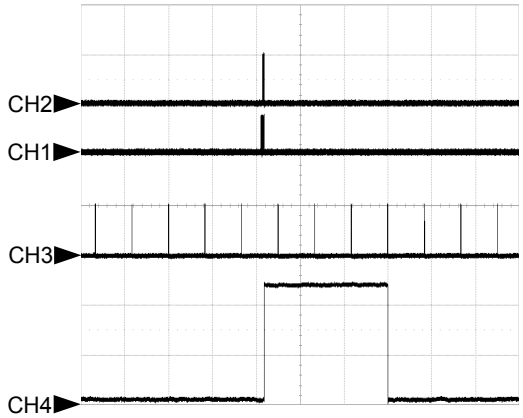
CH1:V_{xFAULT}-5V/div
CH2:$V_{LED\ Drain}$-1V/div
CH3:V_{OUT}-10V/div
CH4:I_{LEDx}-200mA/div
Time:500ms/div

Short LED - Retrial



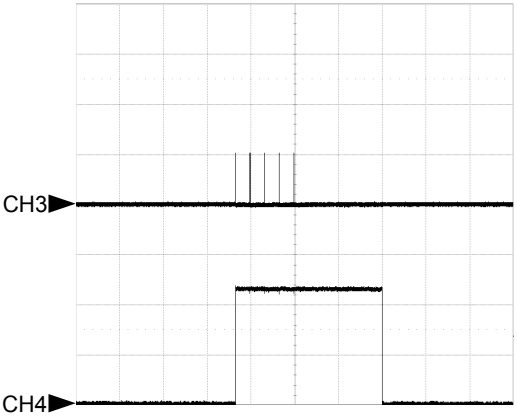
CH1:V_{xFAULT}-5V/div
CH2:$V_{LED\ Drain}$-5V/div
CH3:V_{OUT}-10V/div
CH4:I_{LEDx}-200mA/div
Time:100ms/div

BIST Function – Wait 3 VSYNC



CH1:V_{SDI}-5V/div
CH2:V_{SCL}-5V/div
CH3:V_{SYNC}-5V/div
CH4:I_{LEDx}-50mA/div
Time:20ms/div

VSYNC Detection



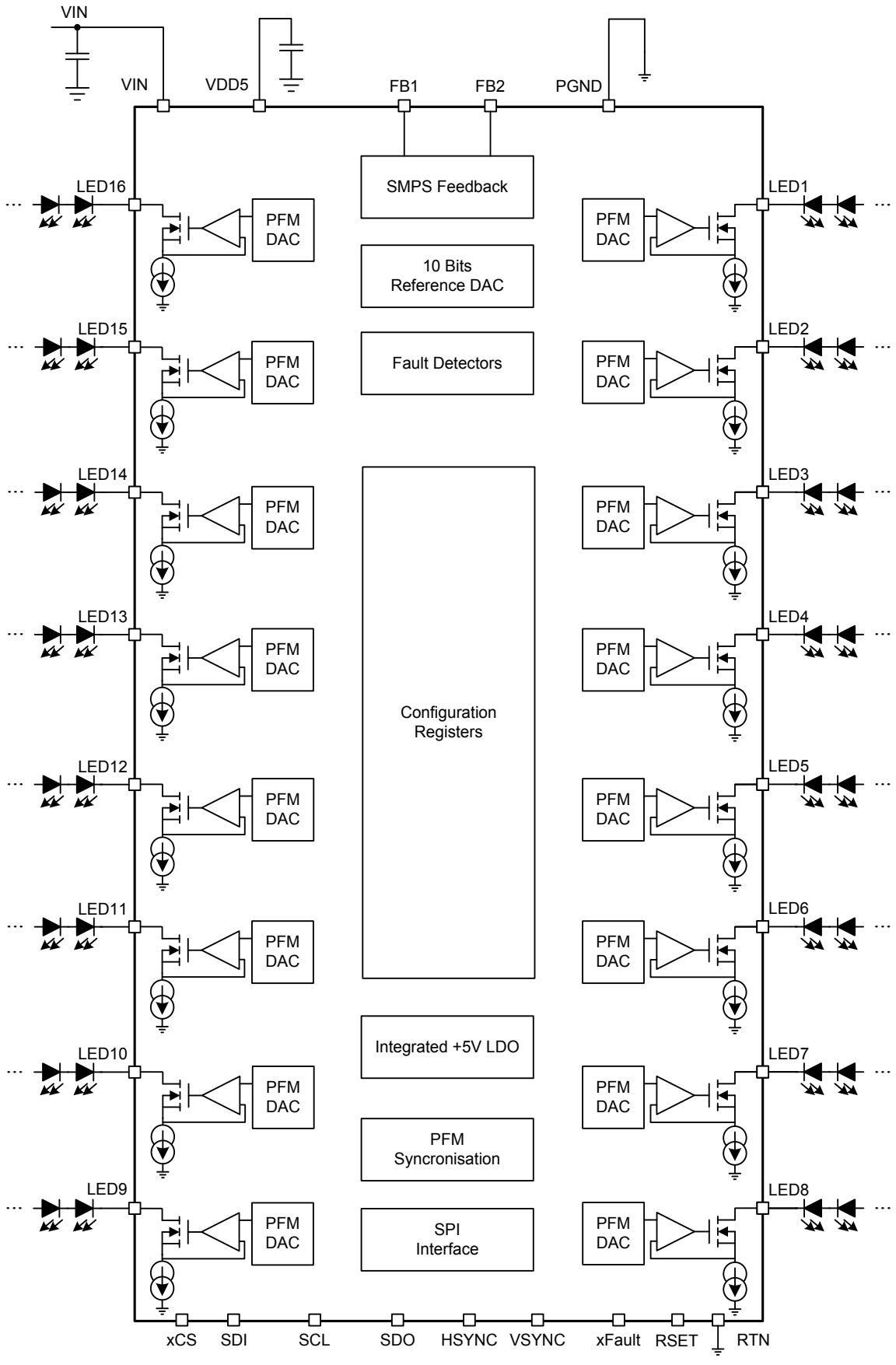
CH1:-
CH2:-
CH3:V_{SYNC}-5V/div
CH4:I_{LEDx}-50mA/div
Time:50ms/div

OperatingWaveforms (Cont.)

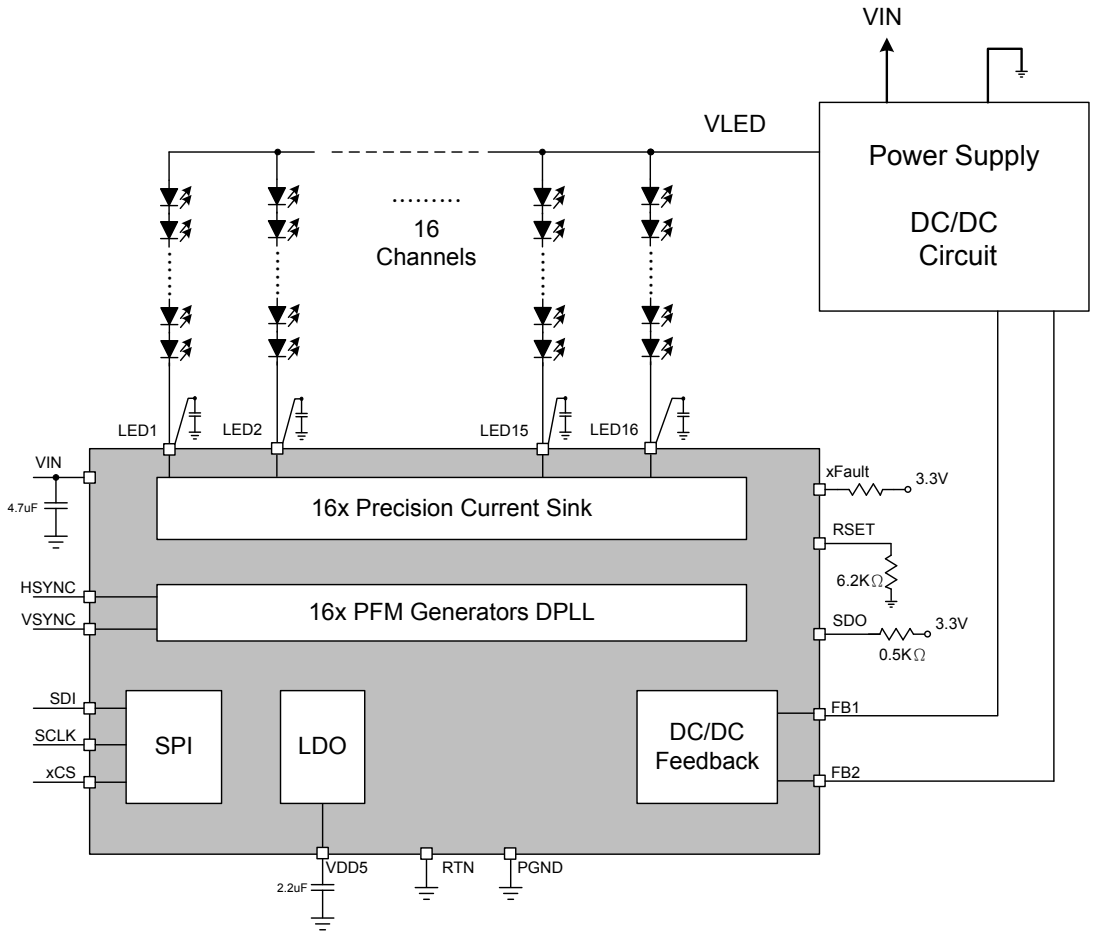
Adaptive Control Function -
disable to enable

CH1:V_{SYNC}-5V/div
CH2:$V_{LED\ Drain}$-2V/div
CH3:V_{SDI}-5V/div
CH4:I_{LEDx}-100mA/div
Time:200ms/div

Block Diagram



Typical Application Circuit



Note 4:When LED1 to 16 of APE5030A pin-out location to external LED string cathode location has execcd 1uH wire inducutance, suggestion add the MLCC capcitors for holdout interference.

Function Descriptions

Power Sequence and UVLO

The APE5030A are integrates Mosfet and 16 channel LED controller for LCD backlight. It's high accurate LED current 1% (120mA LED current) and wide input voltage range.

The APE5030A Using power sequence as below figure 1:

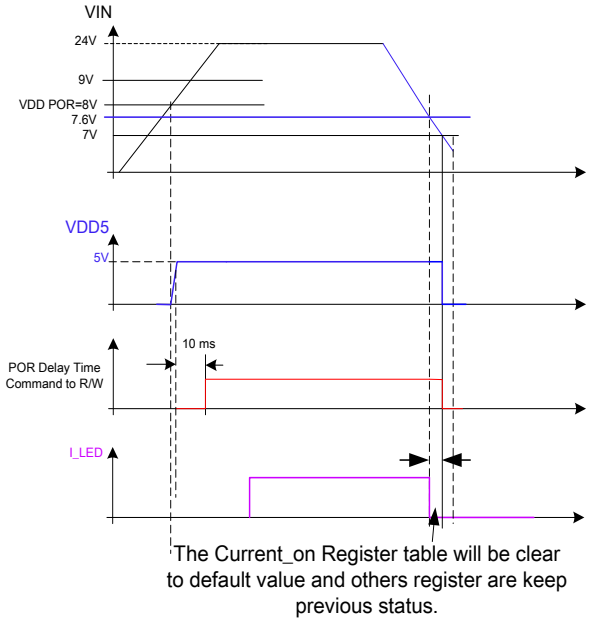


Figure 1: Power Sequence

When VIN supply power voltage exceeds input POR level, the APE5030A will be standby mode status. At this time, the SPI commend can be reading / writing after must waiting 10ms.
The VIN supply power is falling down to 7.6V(typ) then all LED current channels will be shutdown. In the same time; the current on register will be clear to default value and others register are keep previous status. If the VIN supply power voltage was continuous falling down to UVLO=7V (falling) then the APE5030A is shutdown mode.

Table 1: UVLO Register

Address	Bit	Name	Description
03h	[4]	Auto_off_UV	Note 5

Note 5:
Bit [4] =0 ... Under voltage lockout disabled.
Bit [4] =1 ... Under voltage lockout enabled.

If this bit is set to 0 then when the VIN supply voltage is falling down to 7.6V(typ) then LED current is still operation until to VIN voltage is falling down to 7V(typ), the all LED current will be turn off and all register will be clear to default value and IC was shutdown mode. On the contrary; the bit [4] is setting to 1 when the VIN supply power is falling down to 7.6V(typ) then all LED current channels will be shutdown. In the same time; the current_on register will be clear to default value and others register are keep previous status.

LED Short Detection

The APE5030A has LED short detection function, when LED string happen short conditions then APE5030A can detection the abnormal condition. The register address 0x64 bit [2:0] are setting LED string short condition, it's from 3V adjustment to 12V for different LED string application.

Table 2: Short LED Function Register

Address	Bit	Name	Description
64h	[2:0]	Short_level[2:0]	Note 6

Note 6:
Short detection voltage based on drain.
Bit [2:0] =000 ... 3V
Bit [2:0] =001 ... 4V
...
Bit [2:0] =110 ... 9V
Bit [2:0] =111 ... 12V

Function Descriptions (Cont.)

Table 3: Short LED Function Register

Address	Bit	Name	Description
64h	[3]	LED_Short_EN	Note 7

Note 7:
Bit [3] =0 ... Short LED detection disabled
Bit [3] =1 ... Short LED detection enable.

APE5030A LED short detection function is want to enable must using register address 0x64 bit[3]=1 then LED short detection will be enable. On the contrary; the LED short function will be disabling.

Table 4: Short LED Function Register

Address	Bit	Name	Description
64h	[5]	Short_Retrial	Note 8
64h	[4]	Short_auto_off	Note 9

Note 8:
Bit [5] =0 ... short retrial function disable
Bit [5] =1 ... short retrial function enable.
Note 9:
Bit [4] =0 ... short auto-off function disable
Bit [4] =1 ... short auto-off function enable.

APE5030A short LED function has retrial and auto-off behavior. If APE5030A want to enable auto-off function then register address 0x64 bit [3] must is 1 and register address 0x64 bit[4] =1, at this time; the LED1 to LED16 voltage was exceed setting short_level [2:0] then LED channels will be turn off. On the contrary; the LED channels was normal operation.
If short LED function behavior is retrial function then register address 0x64 bit[3] , 0x64 bit[4] and 0x64 bit[5] are setting 1, when LED1 to LED16 voltage was exceed short_level [2:0] then LED channels will be on-off phenomenon, On the contrary; the LED channels were normal operation.

Table 5: retrial time setting Register

Address	Bit	Name	Description
14h	[7:0]	Retrial_Time_L	Note 10
15h	[2:0]	Retrial_Time_H	Note 10

Note 10:
The address 0x15h bit[2:0] and 0x14h bit[7:0] are setting LED open and short LED retrial time, the resolution is per 1ms/LSB.
0x15h bit[2:0]=000, 0x14h bit[7:0]=00000000 ... no retrial time.
0x15h bit[2:0]=000, 0x14h bit[7:0]=00000001 ... 1ms.
0x15h bit[2:0]=000, 0x14h bit[7:0]=00000010 ... 2ms.
...
0x15h bit[2:0]=111, 0x14h bit[7:0]=11001110 ... 1998ms.
0x15h bit[2:0]=111, 0x14h bit[7:0]=11001111 ... 1999ms.

When short LED function was happen and short LED is retrial behavior, the retrial time can be setting and fault times also can be setting by register, see the table 5 and 6.

Table 6: Short LED Function Register

Address	Bit	Name	Description
64h	[7:6]	Short_debouncer	00: 1 fault 01: 6 faults 10: 11 faults 11: 15 faults

Suggestion the APE5030A using the LED short detection must the address register current_on can to 1 after the address 0x64 bit [5:3] is setting finished first.

LED Open Detection

The APE5030A has LED open detection function, when LED string or any LED happen open condition then the APE5030A can detection that abnormal operation.

Table 7: LED Open Function Register

Address	Bit	Name	Description
03h	[1]	LED_Open_EN	Note 11

Note 11:
Bit [1] =0 ... LED Open detection disabled
Bit [1] =1 ... LED Open detection enable.

APE5030A LED open detection function is want to enable must using register address 0x03 bit[3]=1 then LED open detection will be enable. On the contrary; the LED short function will be disabling.

Table 8: LED Open Function Register

Address	Bit	Name	Description
03h	[3]	Retrial_Open	Note 12
03h	[0]	Auto_Off_Open	Note 13

Note 12:
Bit [3] =0 ... retrial open function disable
Bit [3] =1 ... retrial open function enable.
Note 13:
Bit [4] =0 ... auto-off open function disable
Bit [4] =1 ... auto-off open function enable.

Function Descriptions (Cont.)

APE5030A LED open detection function has retrial open and auto-off open behavior. If APE5030A want to enable auto-off open function then register address 0x03 bit [1] must is 1 and register address 0x03 bit[0] =1, at this time; the LEDx voltage was lower than then internal threshold then LEDx channels will be turn off and latch. Even if the LED open failure was eliminate then LEDx channels are not work properly. The auto-off open function sees the figure 2 as below:

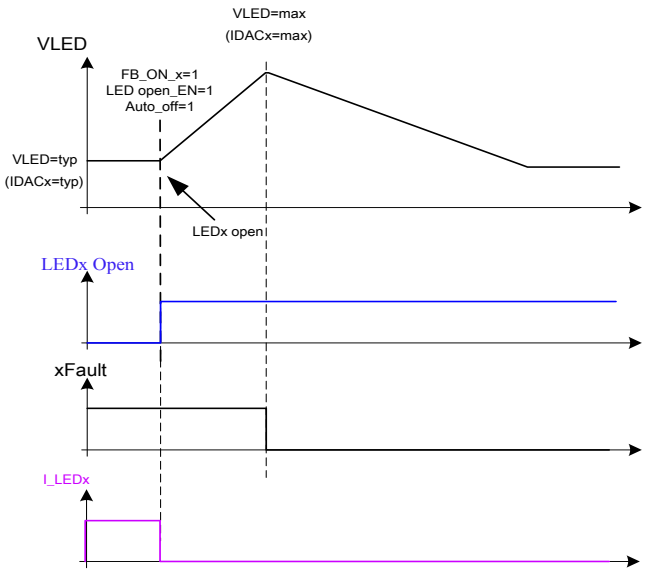


Figure 2: LED open - auto off

If the LED open function is want to retrial behavior, the register address 0x03 bit [1] and 0x03 bit [3] setting to 1. When any LEDx channels are open then IDACx will be increase to max value until to LED open is still existence. The detail LED open retrial behavior sees the figure 3 as below:

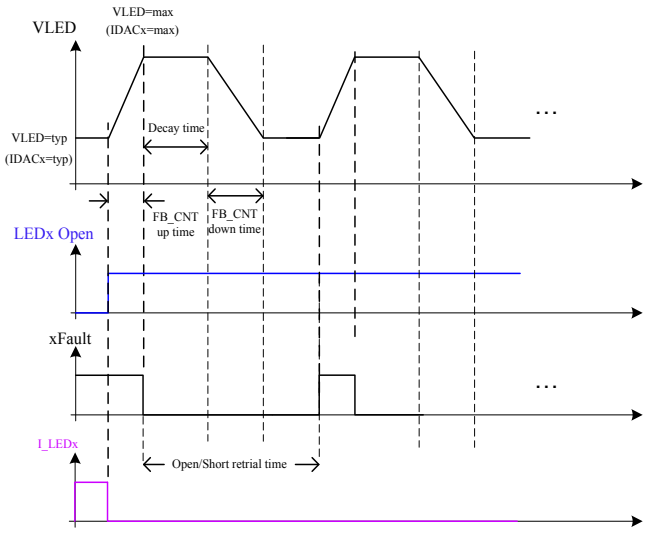


Figure 3: LED open - retrial

The open detection function needs to be combined with the FB function. The open function will be action. Otherwise the open function was not reaction.

OTW and OTP

The APE5030A has OTW and OTP protection function, when APE5030A happen any abnormal operation causes to over temperature until to reach OTP then the xfault pin will be turn low. The table 9 is setting.

Table 9: Auto-off OTP Register

Address	Bit	Name	Description
03h	[2]	Auto_off_OTP	Note 15

Note 15:
Bit [2] =0 ... temperature shutdown disabled.
Bit [2] =1 ... temperature shutdown enable.

The table 9 is setting auto-off OTP, when this bit is setting to 1 then LED current will be turn off when happen OTP condition. On the contrary; the OTP function will be disabling. By the way; when the auto-off OTW and OTW selection was setting then auto-off OTP was not setting to 1 still can be turn off LED current.
Secondly; the address 0x60 bit [4] is detection the OTP fault register. If this bit was written to 1 then OTP happen, On the contrary; the OTP condition is not happen. The same detection function address 0x60 bit [6] is detection OTW function; the function is the same OTP. The address 0x60 bit [6] must cooperate address 0x03 bit [7:6] was setting to 00 to 10 then this bit can be response.

Table 10: OTW Selection Function Register

Address	Bit	Name	Description
03h	[7:6]	OTW Selection	Note 16

Note 16:
Bit [7:6] =00 ... 110°C
Bit [7:6] =01 ... 120°C
Bit [7:6] =10 ... 140°C
Bit [7:6] =11 ... Disable.

The table 10 is setting OTW selection register; it does can be setting different OTW point and OTW function disable.

Table 11: Auto-off OTW Register

Address	Bit	Name	Description
03h	[5]	Auto_off_OTW	Note 17

Note 17:
Bit [5] =0 ... Warning temperature (OTW) shutdown disabled.
Bit [5] =1 ... Warning temperature (OTW) shutdown enabled.

The table 11 is setting auto_off OTW function, when this bit is setting to 1 then the temperature is reaction to OTW point, the LED current will be turn off, on the contrary; then LED current is not turn off.

Function Descriptions (Cont.)

To sum it up the OTW and OTP function; the as below table 12 has OTW and OTP true table can see overall behavior.

Table 12: OTW and OTP true table

Temperature	OTW SEL	OTW	OTP	OTW Fault register	OTP Fault register	LED Current	xFault PIN
Temp >110℃	0	0	0	x	x	x	High
Temp >160℃	0	0	0	x	fault	x	Low
Temp >110℃	0	0	1	x	x	x	High
Temp >160℃	0	0	1	x	fault	shutdown	Low
Temp >110℃	0	1	0	x	x	x	High
Temp >160℃	0	1	0	x	fault	x	Low
Temp >110℃	0	1	1	x	x	x	High
Temp >160℃	0	1	1	x	fault	shutdown	Low
Temp >110℃	1	0	0	fault	x	x	Low
Temp >160℃	1	0	0	fault	fault	x	Low
Temp >110℃	1	0	1	fault	x	x	Low
Temp >160℃	1	0	1	fault	fault	shutdown	Low
Temp >110℃	1	1	0	fault	x	shutdown	Low
Temp >160℃	1	1	0	fault	fault	shutdown	Low
Temp >110℃	1	1	1	fault	x	shutdown	Low
Temp >160℃	1	1	1	fault	fault	shutdown	Low

Adaptive Control Mode

The APE5030A has adaptive control mode function. Its main protection LEDx voltage is over than LED normal operation voltage cause to IC temperature is too high issue.

The adaptive control mode mechanism is mainly used the LEDx voltage over than the setting internal threshold, the LED current will be change to LED current setting multiply by 1.375 times (if need to max ability condition) increase and the LED current on duty will be reducing to the LED current average value is the same before adaptive control mode is not enable. The waveform can see figure 4 as below.

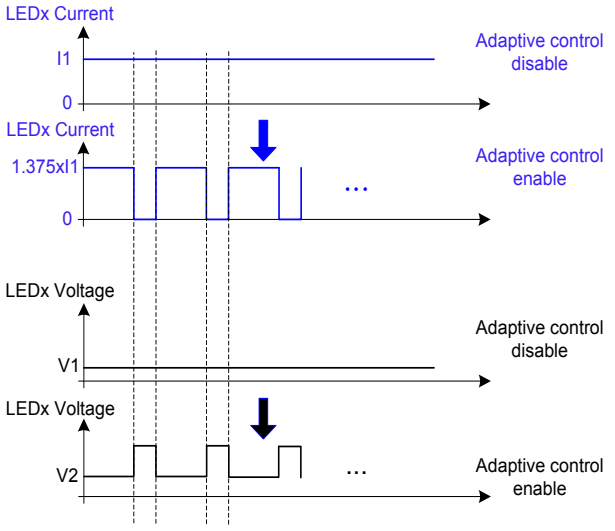


Figure 4: Adaptive Control Mode

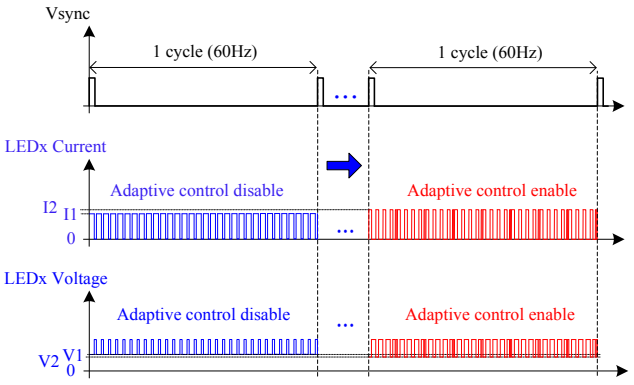


Figure 5: Adaptive Control Mode Example

For example; Using the vsync signal is 60Hz and PFM duty was setting to 75%, in the meantime; the adaptive control function was not enable. When adaptive control function condition already reach then adaptive control function will be enable, see that figure 5. when the adaptive function enable then LED current will be appear to PFM method showing, in the meantime; the LED current peak value will be change and increase the peak current, the PFM duty will be change and decrease, the LED current between enable and disable was not change. The PFM duty and LED current change mechanism will be through the algorithm to realization.

The adaptive control mode enable conditions must include as below condition:
a. Address 0x07 bit [7] is setting to 1.
b. LEDx voltage is more than address 0x07 bit [5:4] value.
c. The setting VADC value is more than address 0x6D and 0x6E value.
d. The setting PFM brightness value is more than address 0x6F and 0x70 values.
e. Vsync signal must exist.

Table 13: ASW_EN Register

Address	Bit	Name	Description
07h	[7]	ASW_EN	Note 18

Note 18:
Bit [7] =0 ... Adaptive control disabled.
Bit [7] =1 ... Adaptive control enabled.

This bit is setting to 1 then adaptive control enable. Otherwise the adaptive control is disabling.

Table 14: Aswitch_VSEL Register

Address	Bit	Name	Description
07h	[5:4]	Aswitch_VSEL	Note 19

Note 19:
Bit [5:4] =00 ... 0.6V.
Bit [5:4] =01 ... 0.8V.
Bit [5:4] =10 ... 0.4V.
Bit [5:4] =11 ... 0.5V.

Function Descriptions (Cont.)

That bits are setting LEDx voltage threshold, when actual LEDx voltage is more than the value then adaptive control will be enable, if LEDx voltage is not exceed this setting then that disable.

Table 15: ASW_VADC_TH Register

Address	Bit	Name	Description
6Dh	[7:0]	ASW_VADC_TH_H[9:2]	-
6Eh	[1:0]	ASW_VADC_TH_L[1:0]	-

0x6Dh bit [7:0] and 0x6Eh bit [1:0] are setting VDAC threshold, when the value is not exceed the VDAC setting (0x0Ch bit [7:0] and 0x0Dh bit [1:0]) then the adaptive control mode is enable. It's the same; if that's value is exceed VDAC setting then disable. In addition; 0x6Dh bit [7:0] and 0x6Eh bit [1:0] resolution is 0.78125mV/bit.

If the DAC code was setting 1 to 495 then the resolution is 1.5625mV/Bit, otherwise; the resolution was 0.78125mV/bit.

Table 16: ASW_Brightness_TH Register

Address	Bit	Name	Description
6Fh	[7:0]	ASW_BRI_TH_L[9:2]	-
70h	[5:0]	ASW_BRI_TH_H[13:8]	-

0x6Fh bit [7:0] and 0x70h bit [5:0] are setting ASW brightness threshold, when the value is the same not exceed the PFM brightness setting (0x37h to 0x65h) then the adaptive control mode is enable. It's the same; if that's value is exceed brightness setting then disable. In addition; 0x6Fh bit [7:0] and 0x70h bit [5:0] resolution is 0.0061%/bit.

Suggestion the APE5030A using adaptive control mode must will be set the condition a to e finished first before current _on can be to 1. Moreover; if the adaptive control mode has occurred before any one of the conditions a to e does not exist, the adaptive controling mode is irreversible. The mean is adaptive control mode has happen, even if the adaptive control mode enable conditions to had any one is not exist; the adaptive control mode was still start up.

PFM mode

The figure 6 is PFM mode mechanism. Its use to 16 sub frame set into one cycle. When the PFM brightness duty is increase, the LED current will also increase. The increase method is using plug-in and sequentially.

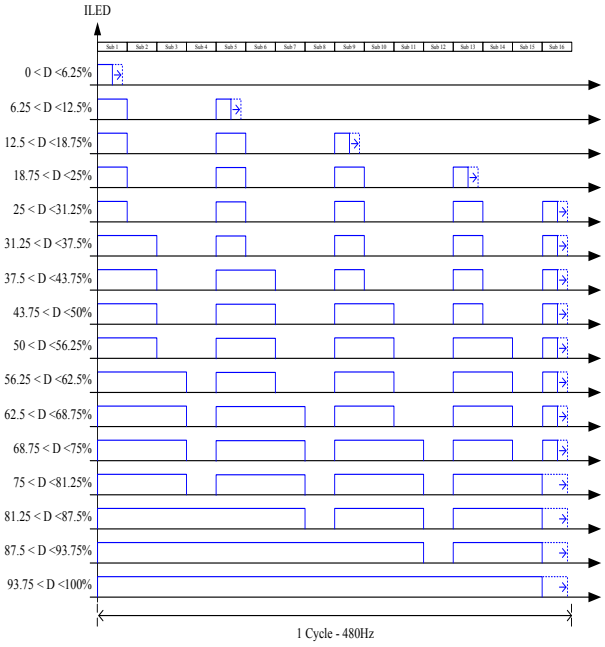


Figure 6: LED current of PFM mode

LEDx channels on/off

The APE5030A has 16 LED channels that can be individually control on/off, see then table 17;

Table 17: LEDx channels on/off Register

Address	Bit	Name	Description
01h	[7:0]	Curr_8 – Curr_1	Note 20
02h	[7:0]	Curr_16 – Curr_9	Note 21

Note 20:
Bit [7:0] =00000000 ... LED8 to LED1 turn off.
Bit [7:0] =00000001 ... LED1 turn on.
Bit [7:0] =00000010 ... LED2 turn on.
...
Bit [7:0] =01000000 ... LED7 turn on.
Bit [7:0] =10000000 ... LED8 turn on.
Every bit is control individually LED channel on/off.
Note 21:
Bit [7:0] =00000000 ... LED16 to LED9 turn off.
Bit [7:0] =00000001 ... LED9 turn on.
Bit [7:0] =00000010 ... LED10 turn on.
...
Bit [7:0] =01000000 ... LED15 turn on.
Bit [7:0] =10000000 ... LED16 turn on.
Every bit is control individually LED channel on/off.

Function Descriptions (Cont.)

VDAC Adjustment

The APE5030A include 10 bits VDAC code, it's provide user can be adjustment the voltage and then adjustment LED current. The every bit correspond VDAC code voltage and LED current as below table 18:

Suggestion the write the VDAC code sequences as below: First writing address 0x0D and then writing address 0x0C, the VDAC data will be update.

Table 18: VDAC Correspondence table

Bit(dec)	VDAC (mV)	LED current (mA)
1	1.5625	~0.252
79	123.44	20
476	743.8	120
496	775	125
497	388.28	125.244
992	775	250

In addition; the address 0x0C and 0x0D are setting VDAC code, see the table19.

Table 19: VDAC Register

Address	Bit	Name	Description
0Ch	[7:0]	VDAC[9:2]	-
0Dh	[1:0]	VDAC[1:0]	-

This is simple calculation formula for V_{DAC} exchange to I_{LED} (mA).If the register DAC_Code values are from 1 to 496 then V_{DAC} and I_{LED} formula equal as below:

V_{DAC} (mV) = 2*(800mV/1024)*DAC_Code
I_{LED} (mA) = (VDAC/6.2K)*1000

When the registrer DAC_Code values more than 497 then V_{DAC} and I_{LED} formula equal as below:

V_{DAC} (mV) = (800mV/1024)*DAC_Code
I_{LED} (mA) = (VDAC/6.2K)*2000

Dual Channels Control

The address 0x13h bit [7] is setting dual channels function. The mainly effect is even channel LED current follow odd channel LED current.

Table 20: Dual Channels Register

Address	Bit	Name	Description
13h	[7]	Dual_channel	Note 22

Note 22:
Two channel combine: even number channel control by odd channel (EX, ch2 PFM output = ch1 PFM output):
Bit [7] =0 ... disable.
Bit [7] =1 ... enable.

If dual channel function is wants to using then address 0x13h bit [7] must setting to 1 and the PFM brightness also must setting. Finally; the current on register can be turn on.
Suggestion the registers were setting; the registers value should not be adjusted.

PFM Delay and PFM Brightness

The address 0x16 to 0x35 is setting PFM delay time. It's has 12 bits resolution can adjustment LED1 to LED16. Secondly PFM delay function must cooperation VSYNC can be working. The register sees the register map.
The address 0x37 to 0x56 is setting PFM brightness. It's has 14 bits resolution can adjustment LED1 to LED16. the resolution is approximate 0.061%/LSB. Suggestion using the PFM brightness range is from 1% to 100%.

Decay Time

In order to auto adjustment optima output voltage by external circuit, it need to detect time and function. The table 21 is setting detection enable/disable. The detect time can be adjustment range from 32ms change to 128ms.

Suggestion the registers were setting; the registers value should not be adjusted.

Table 21: FB decay enable/disable Register

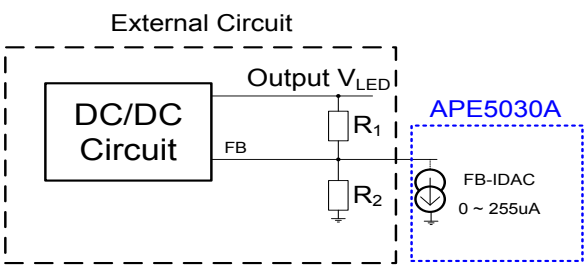
Address	Bit	Name	Description
66h	[7]	Fb2_decay_off	Note 23
66h	[6]	Fb1_decay_off	Note 24

Note 23:
Bit [7] =0 ... FB counter2 decay time is enable and defined by register decay_time.
Bit [7] =1 ... FB counter2 decay time is disable.
Note 24:
Bit [6] =0 ... FB counter1 decay time is enable and defined by register decay_time.
Bit [6] =1 ... FB counter1 decay time is disable.

Dynamic Feedback Control

The APE5030A has FB1 and FB2 terminal can be connect to feedback pin of external DC/DC circuit and control output voltage (V_{LED}) for optimal power efficiency.

The dynamic control mechanism is according to output voltage is not enough condition and then increasing the FB-IDAC value, at the same time; output voltage also increase until to LED current achieve target.
In order to simplify design step, a few process step provide calculate and design as below:



Function Descriptions (Cont.)

Step 1: Calculate R1

The output voltage is depending on min to max range of LED. Design the R1 value according to with max IDAC value 255uA as below formula:

$$R_1 = \frac{V_{LED(MAX)} - V_{LED(MIN)}}{255uA}$$

Suggestion the R1 value multiply by IDAC current max value is not more than over voltage protection point of external DC/DC circuit. Otherwise; when the IDAC value is increasing to max value then happen protection of external DC/DC circuit. Secondly; the LED output voltage max to min range must according to actual LED specification.

Step 2: Calculate R2

The R2 value calculates as below formula:

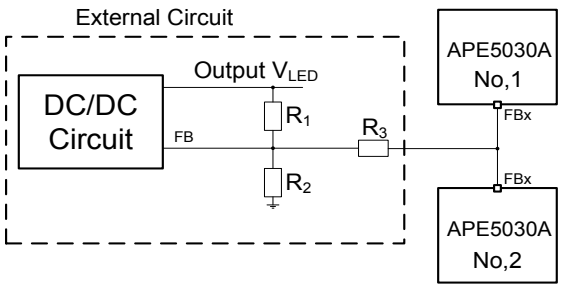
$$R_2 = \frac{R_1}{(\frac{V_{LED(MIN)}}{V_{FB}} - 1)}$$

The APE5030A using automatic mode and manual mode can be adjustment FB-IDAC current. If adjustment mode is choose the manual mode then using address 0x12 bit [5] and bit [4] setting to 1 and increasing the address 0x10 and 0x11 bit value so that increasing output voltage. According to formula as below:

$$V_{LED} = (1 + \frac{R_1}{R_2}) \times V_{FB} + R_1 \times IDAC_{(COUTER)} \times 1uA$$

If one DC/DC converter is connected 2 or more than APE5030A structure suggest series resistor between FBx terminal and DC/DC circuit feedback terminal let FBx current can up to 255uA. The R3 value calculates as below:

$$R_3 = \frac{V_{FB}}{255uA}$$



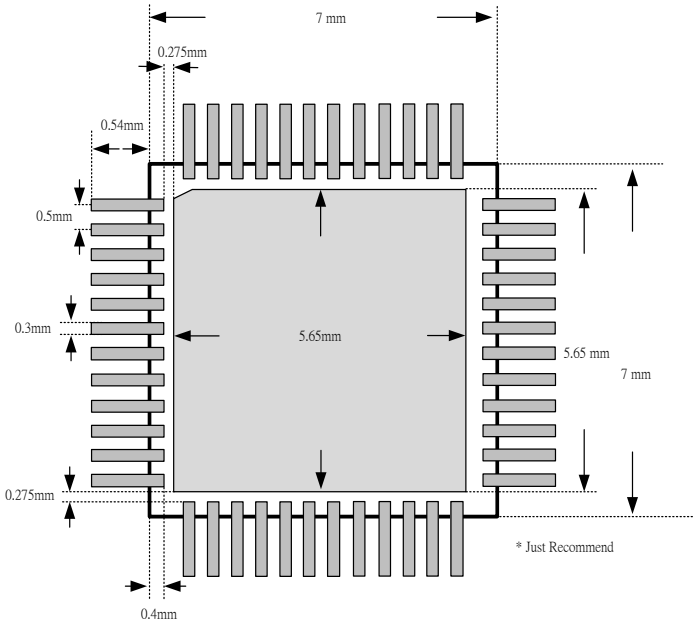
If possible; try to let FBx pin terminal keep to 0.25V and it's not less than 0.25V.

Application Information

Layout Consideration

The APE5030A was using less external components. Suggestion the RSET, input capacitor and VDD5 capacitor are as possible closed to IC terminal.
If using APE5030A the layout consideration can be seen as below figure. When LED current was larges can cause to thermal issue, suggestion using to via then solve the thermal issue.
The holes and via numbers can be effect to thermal, if using holes and via are more, the thermal issue will be decreasing.
Thermal problem can using as below points can decrease the thermal issue:
1. Increasing the PCB dimension and add the copper plating of ground side areas.
2. If possible, the PCB layers suggest using 4 layers or more than layer is better.
3. Using the holes size and via connect to all layers and then decrease the thermal issue.
To sum it up, according to as be above points, the thermal issue will be effective decreasing and solution.

Minimum Footprint



QFN 7x7 - 48

Register Map

Register Address (hex)	Name	BIT	Label	Default	Description
0x01	CUR_ON_1	[7:0]	curr_8 - curr_1	1111_1111	output drivers 8-1: 0: output driver disabled **1: output driver enabled**
0x02	CUR_ON_2	[7:0]	curr_16 - curr_9	1111_1111	output drivers 16-9: 0: output driver disabled **1: output driver enabled**
0x03	FAULT_1	[7:6]	OTW_SEL	11	OTW pin configuration: 00:110 °C 01:120 °C 10:140 °C **11:disable**
		[5]	auto_off_OTW	1	0: Warning temperature (OTW) shutdown disabled **1: Warning temperature (OTW) shutdown enabled**
		[4]	auto_off_uv	1	0: Under voltage lockout disabled **1: Under voltage lockout enabled, if VDD <VDD_UVL all channels are turned off by resetting CURRx-bits.**
		[3]	retrial_open	1	0: open LED retrial function disabled **1: open LED retrial function enabled**
		[2]	auto_off_OTP	1	0: temperature shutdown disabled **1: temperature shutdown enabled**
		[1]	open_en	1	0: open LED detection disabled **1 : open LED detection for all channels enabled**
		[0]	auto_off_open	1	Automatic feedback turn off in case of open LED: 0: feedback function of open LED channel enabled **1 : feedback function of open LED channel automatically disabled**
0x04	GPIO_CTRL	[7:6]	fault_io_config[1:0]	00	xFault pin configuration: **00: Open Drain / Pulldown** 01: Push - Pull 10: Disabled (HIZ) 11: not used
		[5:4]	SDO_io_config[1:0]	01	SDO pin configuration: 00: Open Drain / Pull down **01: Push - Pull** 10: Disabled (HI-Z) 11: Not used
0x05	FB_SEL_1	[7]	fb_sel_8	0	select FB channel for current outputs 8: **0: select FB pin FB1** 1: select FB pin FB2

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x05	FB_SEL_1	[6]	fb_sel_7	0	select FB channel for current outputs 7: **0: select FB pin FB1** 1: select FB pin FB2
		[5]	fb_sel_6	0	select FB channel for current outputs 6: **0: select FB pin FB1** 1: select FB pin FB2
		[4]	fb_sel_5	0	select FB channel for current outputs 5: **0: select FB pin FB1** 1: select FB pin FB2
		[3]	fb_sel_4	0	select FB channel for current outputs 4: **0: select FB pin FB1** 1: select FB pin FB2
		[2]	fb_sel_3	0	select FB channel for current outputs 3: **0: select FB pin FB1** 1: select FB pin FB2
		[1]	fb_sel_2	0	select FB channel for current outputs 2: **0: select FB pin FB1** 1: select FB pin FB2
		[0]	fb_sel_1	0	select FB channel for current outputs 1: **0: select FB pin FB1** 1: select FB pin FB2
0x06	FB_SEL_2	[7]	fb_sel_16	0	select FB channel for current outputs 16: **0: select FB pin FB1** 1: select FB pin FB2
		[6]	fb_sel_15	0	select FB channel for current outputs 15: **0: select FB pin FB1** 1: select FB pin FB2
		[5]	fb_sel_14	0	select FB channel for current outputs 14: **0: select FB pin FB1** 1: select FB pin FB2
		[4]	fb_sel_13	0	select FB channel for current outputs 13: **0: select FB pin FB1** 1: select FB pin FB2
		[3]	fb_sel_12	0	select FB channel for current outputs 12: **0: select FB pin FB1** 1: select FB pin FB2
		[2]	fb_sel_11	0	select FB channel for current outputs 11: **0: select FB pin FB1** 1: select FB pin FB2
		[1]	fb_sel_10	0	select FB channel for current outputs 10: **0: select FB pin FB1** 1: select FB pin FB2
		[0]	fb_sel_9	0	select FB channel for current outputs 9: **0: select FB pin FB1** 1: select FB pin FB2

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x07	CURR_CTRL	[7]	ASW_EN	0	Adaptive control disable / enable : **0: Disable** 1: Enable
		[5:4]	Aswitch_vsel	00	reference voltage for adaptive control configuration: **00: 0.6V** 01: 0.8V 10: 0.4V 11: 0.5V
		[3]	phase_shift	0	**0: phase shift on/off depends on register direct_pwm** 1: phase shift is turned on (VSYNC must be selected as PFM source)
		[2]	Cgate_ compensation	1	Current output pre-charge compensation 0: off **1: High Time counter is started when external FET has reached its threshold voltage**
		[1:0]	slew_rate	11	Defines the slew rate of the output stage 00: 250mV / 16us 01: 250mV / 8us 10: 250mV / 4us **11: Full speed**
0x08	FAULT_SHORT_1	[7]	ShortLED_8	0	Short LED detected on output 8-1: Read: 0: no short LED detected 1: Short LED detected Write: 1: clear fault
		[6]	ShortLED_7	0	
		[5]	ShortLED_6	0	
		[4]	ShortLED_5	0	
		[3]	ShortLED_4	0	
		[2]	ShortLED_3	0	
		[1]	ShortLED_2	0	
		[0]	ShortLED_1	0	
0x09	FAULT_SHORT_2	[7]	ShortLED_16	0	Short LED detected on output 16-9: Read: 0: no short LED detected 1: Short LED detected Write: 1: clear fault
		[6]	ShortLED_15	0	
		[5]	ShortLED_14	0	
		[4]	ShortLED_13	0	
		[3]	ShortLED_12	0	
		[2]	ShortLED_11	0	
		[1]	ShortLED_10	0	
		[0]	ShortLED_9	0	

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0A	OPENLED_1	[7]	OpenLED_8	0	Open LED detected on output 8-1: Read: 0: no open LED detected 1: Open LED detected Write: 1: clear fault
		[6]	OpenLED_7	0	
		[5]	OpenLED_6	0	
		[4]	OpenLED_5	0	
		[3]	OpenLED_4	0	
		[2]	OpenLED_3	0	
		[1]	OpenLED_2	0	
		[0]	OpenLED_1	0	
0x0B	OPENLED_2	[7]	OpenLED_16	0	Open LED detected on output 16-9: Read: 0: no open LED detected 1: Open LED detected Write: 1: clear fault
		[6]	OpenLED_15	0	
		[5]	OpenLED_14	0	
		[4]	OpenLED_13	0	
		[3]	OpenLED_12	0	
		[2]	OpenLED_11	0	
		[1]	OpenLED_10	0	
		[0]	OpenLED_9	0	
0x0C	VDAC_H	[7:0]	VDAC[9:2]	0111_0111	MSB - BITS OF 10 bit VDAC
0x0D	VDAC_L	[1:0]	VDAC[1:0]	00	LSB - BITS OF 10 bit VDAC
0x0E	FB_ON_1	[7:0]	FB_CURR_8–FB_CURR_1	1111_1111	Enables feedback function of output channels: 0: feedback function of selected channel disabled **1: feedback function of selected channel enabled**
0x0F	FB_ON_2	[7:0]	FB_CURR_16–FB_CURR_9	1111_1111	Enables feedback function of output channels: 0: feedback function of selected channel disabled **1: feedback function of selected channel enabled**
0x10	IDAC_FB1_COUNTER	[7:0]	IDAC_FB1_counter	0000_0000	Feedback counter (IDAC) 1 value **0x00: FB-current 0μA** 0xFF: FB-current 255μA Value can be overwritten if Fb_cnt_man_fb1=1
0x11	IDAC_FB2_COUNTER	[7:0]	IDAC_FB2_counter	0000_0000	Feedback counter (IDAC) 2 value **0x00: FB-current 0μA** 0xFF: FB-current 255μA Value can be overwritten if Fb_cnt_man_fb2=1

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x12	FBLOOP_CTRL	[7:6]	Vtrip[1:0]	00	Select gate voltage threshold for feedback function: **00: (VDD/8)*7** 01: (VDD/8)*6 10: (VDD/8)*5 11: (VDD/8)*4
		[5]	FB_cnt_man_fb2	0	**0: FB2 counter in automatic mode** 1: FB2 counter is set manually
		[4]	FB_cnt_man_fb1	0	**0: FB1 counter in automatic mode** 1: FB1 counter is set manually
		[3:2]	Fbcount_dn_time[1:0]	01	FB1 and FB2 down counting step time: 00: 512us **01: 2048us** 10: 4096us 11: 8192us
		[1:0]	Fbcount_up_time[1:0]	01	FB1 and FB2 up counting step time: 00: 1024μs **01: 256μs** 10: 64μs 11: 16us
0x13	PFMCTRL	[7]	dual_channel	0	two channel combine : even number channel control by odd channel (EX, ch2 PFM output = ch1 PFM output) **0: disable** 1: enable
		[6]	ClockSrc1	0	Clock source for internal PFM generators **0: internal RC oscillator or HSYNC (depending on ClockSrc0)** 1: DPLL output
		[5]	ClockSrc0	0	Clock source for internal PFM generators **0: internal RC oscillator** 1: external pin HSYNC
		[4]	pfm_rev	0	**0: normal PFM operation** 1: PFM signals are inverted Note: High time becomes Low Time

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x13	PFMCTRL	[3]	vsync_detect	0	**0: VSYNC detection disabled** 1: VSYNC detection enabled All outputs are turned off if VSYNC signal is missing for 100ms.
		[2]	vsync_edge	0	Defines VSYNC trigger edge: **0: trigger on rising edge of VSYNC** 1: trigger on falling edge of VSYNC
		[1]	direct_pwm	1	Select external (PWM signal) or internal PFM signal (frequence range = 60Hz~ 40KHz) 0: PFM signal is generated internally **1: PWM signal is applied externally at pin VSYNC**
		[0]	update_mode	0	Defines when PFM registers are updated: **0: Registers updated with rising edge of xCS** 1: Registers updated with next VSYNC-edge
0x14	RETRIAL_TIME_L	[7:0]	retrial_time[7:0]	1100_1111	Open LED or Short LED Retrial Time (1ms / LSB) 10'h001 : 1ms 10'h002 : 2ms 10'h003 : 3ms … 10'h3CF : 1.999s
0x15	RETRIAL_TIME_H	[2:0]	retrial_time[10:8]	111	
0x16	PFM1delLSB	[7:0]	PFM1del[7:0]	0000_0000	PFM1 Delay LSB
0x17	PFM1delMSB	[3:0]	PFM1del[11:8]	0000	PFM1 Delay MSB
0x18	PFM2delLSB	[7:0]	PFM2del[7:0]	0000_0000	PFM2 Delay LSB
0x19	PFM2delMSB	[3:0]	PFM2del[11:8]	0000	PFM2 Delay MSB
0x1A	PFM3delLSB	[7:0]	PFM3del[7:0]	0000_0000	PFM3 Delay LSB
0x1B	PFM3delMSB	[3:0]	PFM3del[11:8]	0000	PFM3 Delay MSB
0x1C	PFM4delLSB	[7:0]	PFM4del[7:0]	0000_0000	PFM4 Delay LSB
0x1D	PFM4delMSB	[3:0]	PFM4del[11:8]	0000	PFM4 Delay MSB
0x1E	PFM5delLSB	[7:0]	PFM5del[7:0]	0000_0000	PFM5 Delay LSB
0x1F	PFM5delMSB	[3:0]	PFM5del[11:8]	0000	PFM5 Delay MSB
0x20	PFM6delLSB	[7:0]	PFM6del[7:0]	0000_0000	PFM6 Delay LSB
0x21	PFM6delMSB	[3:0]	PFM6del[11:8]	0000	PFM6 Delay MSB
0x22	PFM7delLSB	[7:0]	PFM7del[7:0]	0000_0000	PFM7 Delay LSB
0x23	PFM7delMSB	[3:0]	PFM7del[11:8]	0000	PFM7 Delay MSB
0x24	PFM8delLSB	[7:0]	PFM8del[7:0]	0000_0000	PFM8 Delay LSB

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x25	PFM8delMSB	[3:0]	PFM8del[11:8]	0000	PFM8 Delay MSB
0x26	PFM9delLSB	[7:0]	PFM9del[7:0]	0000_0000	PFM9 Delay LSB
0x27	PFM9delMSB	[3:0]	PFM9del[11:8]	0000	PFM9 Delay MSB
0x28	PFM10delLSB	[7:0]	PFM10del[7:0]	0000_0000	PFM10 Delay LSB
0x29	PFM10delMSB	[3:0]	PFM10del[11:8]	0000	PFM10 Delay MSB
0x2A	PFM11delLSB	[7:0]	PFM11del[7:0]	0000_0000	PFM11 Delay LSB
0x2B	PFM11delMSB	[3:0]	PFM11del[11:8]	0000	PFM11 Delay MSB
0x2C	PFM12delLSB	[7:0]	PFM12del[7:0]	0000_0000	PFM12 Delay LSB
0x2D	PFM12delMSB	[3:0]	PFM12del[11:8]	0000	PFM12 Delay MSB
0x2E	PFM13delLSB	[7:0]	PFM13del[7:0]	0000_0000	PFM13 Delay LSB
0x2F	PFM13delMSB	[3:0]	PFM13del[11:8]	0000	PFM13 Delay MSB
0x30	PFM14delLSB	[7:0]	PFM14del[7:0]	0000_0000	PFM14 Delay LSB
0x31	PFM14delMSB	[3:0]	PFM14del[11:8]	0000	PFM14 Delay MSB
0x32	PFM15delLSB	[7:0]	PFM15del[7:0]	0000_0000	PFM15 Delay LSB
0x33	PFM15delMSB	[3:0]	PFM15del[11:8]	0000	PFM15 Delay MSB
0x34	PFM16delLSB	[7:0]	PFM16del[7:0]	0000_0000	PFM16 Delay LSB
0x35	PFM16delMSB	[3:0]	PFM16del[11:8]	0000	PFM16 Delay MSB
0x37	PFM1brLSB	[7:0]	PFM1BR[7:0]	0000_0000	14'h0001 : 0.0061% 14'h0002 : 0.0122% 14'h0003 : 0.0183% .. 14'h3FFF : 100% PFMBR/16383*100= Brightness percentage
0x38	PFM1brMSB	[5:0]	PFM1BR[13:8]	00_0000	
0x39	PFM2brLSB	[7:0]	PFM2BR[7:0]	0000_0000	PFM2 Brightness LSB
0x3A	PFM2brMSB	[5:0]	PFM2BR[13:8]	00_0000	PFM2 Brightness MSB
0x3B	PFM3brLSB	[7:0]	PFM3BR[7:0]	0000_0000	PFM3 Brightness LSB
0x3C	PFM3brMSB	[5:0]	PFM3BR[13:8]	00_0000	PFM3 Brightness MSB
0x3D	PFM4brLSB	[7:0]	PFM4BR[7:0]	0000_0000	PFM4 Brightness LSB
0x3E	PFM4brMSB	[5:0]	PFM4BR[13:8]	00_0000	PFM4 Brightness MSB
0x3F	PFM5brLSB	[7:0]	PFM5BR[7:0]	0000_0000	PFM5 Brightness LSB
0x40	PFM5brMSB	[5:0]	PFM5BR[13:8]	00_0000	PFM5 Brightness MSB
0x41	PFM6brLSB	[7:0]	PFM6BR[7:0]	0000_0000	PFM6 Brightness LSB
0x42	PFM6brMSB	[5:0]	PFM6BR[13:8]	00_0000	PFM6 Brightness MSB
0x43	PFM7brLSB	[7:0]	PFM7BR[7:0]	0000_0000	PFM7 Brightness LSB
0x44	PFM7brMSB	[5:0]	PFM7BR[13:8]	00_0000	PFM7 Brightness MSB
0x45	PFM8brLSB	[7:0]	PFM8BR[7:0]	0000_0000	PFM8 Brightness LSB
0x46	PFM8brMSB	[5:0]	PFM8BR[13:8]	00_0000	PFM8 Brightness MSB
0x47	PFM9brLSB	[7:0]	PFM9BR[7:0]	0000_0000	PFM9 Brightness LSB
0x48	PFM9brMSB	[5:0]	PFM9BR[13:8]	00_0000	PFM9 Brightness MSB
0x49	PFM10brLSB	[7:0]	PFM10BR[7:0]	0000_0000	PFM10 Brightness LSB
0x4A	PFM10brMSB	[5:0]	PFM10BR[13:8]	00_0000	PFM10 Brightness MSB
0x4B	PFM11brLSB	[7:0]	PFM11BR[7:0]	0000_0000	PFM11 Brightness LSB
0x4C	PFM1brMSB	[5:0]	PFM11BR[13:8]	00_0000	PFM11 Brightness MSB
0x4D	PFM12brLSB	[7:0]	PFM12BR[7:0]	0000_0000	PFM12 Brightness LSB

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x4E	PFM12brMSB	[5:0]	PFM12BR[13:8]	00_0000	PFM12 Brightness MSB
0x4F	PFM13brLSB	[7:0]	PFM13BR[7:0]	0000_0000	PFM13 Brightness LSB
0x50	PFM13brMSB	[5:0]	PFM3BR[13:8]	00_0000	PFM13 Brightness MSB
0x51	PFM14brLSB	[7:0]	PFM14BR[7:0]	0000_0000	PFM14 Brightness LSB
0x52	PFM14brMSB	[5:0]	PFM14BR[13:8]	00_0000	PFM14 Brightness MSB
0x53	PFM15brLSB	[7:0]	PFM15BR[7:0]	0000_0000	PFM15 Brightness LSB
0x54	PFM15brMSB	[5:0]	PFM15BR[13:8]	00_0000	PFM15 Brightness MSB
0x55	PFM16brLSB	[7:0]	PFM16BR[7:0]	0000_0000	PFM16 Brightness LSB
0x56	PFM16brMSB	[5:0]	PFM16BR[13:8]	00_0000	PFM16 Brightness MSB
0x57	ASICIDLSB	[7:4]	asic_id[3:0]	0011	Device ID of APE5030A LSB
		[3:0]	revision[3:0]	0000	Version of APE5030A
0x58	ASICIDMSB	[7:0]	asic_id[11:4]	0101_0000	Device ID of APE5030A MSB
0x59	POWER_CTRL	[0]	Standby	0	Standby power - saving power 0:normal operation 1:Analog circuit power off (MOS) and digital circuit gating clock
0x60	STATUS	[7]	CLKDCO_LOCK	0	1: notify Clock DCO frequency lock
		[6]	STAT OTW	0	1: notify over temperature warning
		[5]	STAT novsync	0	1: notify VSYNC is missing >100ms
		[4]	STAT ov_temp	0	1: notify over temperature fault
		[3]	STAT open	0	1: notify open LED fault
		[2]	Short LED	0	1: notify short LED fault
		[1]	Short BIST	0	1: notify short BIST fault
		[0]	Power Good	0	0: no power supply 1: device ok
0x61	BIST_SHORT_1	[7]	BIST_Short_8	0	Short LED detected with BIST on output 8-1 Read: 0: no short LED detected 1: Short LED detected Write: 1: clear fault
		[6]	BIST_Short_7	0	
		[5]	BIST_Short_6	0	
		[4]	BIST_Short_5	0	
		[3]	BIST_Short_4	0	
		[2]	BIST_Short_3	0	
		[1]	BIST_Short_2	0	
		[0]	BIST_Short_1	0	
0x62	BIST_SHORT_2	[7]	BIST_Short_16	0	Short LED detected with BIST on output 16-9 Read: 0: no short LED detected 1: Short LED at detected Write: 1: clear fault
		[6]	BIST_Short_15	0	
		[5]	BIST_Short_14	0	
		[4]	BIST_Short_13	0	
		[3]	BIST_Short_12	0	
		[2]	BIST_Short_11	0	
		[1]	BIST_Short_10	0	
		[0]	BIST_Short_9	0	
0x63	BIST_CONTROL1	[5]	BIST_EN_2	0	Short BIST enable for FB2: **0: BIST disabled** 1: Start shortled BIST2 test

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x63	BIST_CONTROL1	[4]	BIST_EN_1	0	Short BIST enable for FB1: **0: BIST disabled** 1: Start shortled BIST1 test
		[3]	BIST_fast_time	0	short BIST up/down time step **0: 64uS** 1: 128uS
		[2]	BISTsel_time	0	**0: use bist_fast_time register value** 1: use fbcounter_up_time / fbcounter_dn_time register values
		[1:0]	BIST_wait[1:0]	10	Wait after BIST target has been reached: 0: no wait 01: wait 1 VSYNC pulse **10: wait 2 VSYNC pulses** 11: wait 3 VSYNC pulses
0x64	SHORT_COMP_ CTRL1	[7:6]	short_debouncer[1:0]	11	00: 1 fault 01: 6 faults 10: 11 faults **11: 15 faults**
		[5]	Short_retrial	1	0: retrial function disabled **1: retrial function enabled** **Note: channels turned on every second**
		[4]	Short_auto_off	1	0: automatic turn off function disabled **1: automatic turn off channels of shorted group**
		[3]	LED_short_en	1	0: short LED detection disabled **1 : short LED detection for all channels enabled**
		[2:0]	Short_level[2:0]	000	Short detection voltage based on LEDx voltage. **000…3V** 100…7V 001…4V 101…8V 010…5V 110…9V 011…6V 111…12V

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x65	BRI_MINI	[7:0]	BRI_MINI	0010_1000	if PFM Brightness[7:0] < Mini Brightness[7:0] Mini Brightness[7:0] replace PFM Brightness[7:0] Ex. PFMBR[13:0] = 14'h0005, BRI_MINI[7:0] = 8'h10 => BRI_MINI_ ON = 1, PFMBR[13:0] = 14'h0010
0x66	HDR_mode	[7]	fb2_decay_off	0	**0: FB counter 2 decay time is defined by register decay_time** 1: FB counter 2 decay time is infinite as long all high times in FB group 2 are 0
		[6]	fb1_decay_off	0	**0: FB counter 1 decay time is defined by register decay_time** 1: FB counter 1 decay time is infinite as long all high times in FB group 1 are 0
		[4]	BRI_MINI_ON	0	DUTY minimum enable (depend on 0x65) **0: disable** 1: enable
		[3]	-	-	-
		[2:1]	FBcount_decay_time[1:0]	11	Decay time for power feedback control 00: 32ms 01: 32ms 10: 64ms **11: 128ms**
		[0]	sw_reset	0	Software reset **0: normal operation** 1: software reset bit (registers 0x01 to 0x6C clear to default)

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x69	COMP_REG1	[7:0]	CompReg1–CompReg8	0000_0000	Status of gate trip voltage comparator: **0: Vgate < Vtrip** 1: Vgate > Vtrip
0x6A	COMP_REG2	[7:0]	CompReg9–CompReg16	0000_0000	Status of gate trip voltage comparator: **0: Vgate < Vtrip** 1: Vgate > Vtrip
0x6B	BIST_IDAC1	[7:0]	BT1	1111_1111	Defines the IDAC1 target value for BIST
0x6C	BIST_IDAC2	[7:0]	BT2	1111_1111	Defines the IDAC2 target value for BIST
0x6D	ASW_VADC_TH_H	[7:0]	ASW_VDAC_TH[9:2]	1111_1000	MSB - BITS OF 10 bit Adaptive control VDAC Threshold (0.78125mV/ LSB)
0x6E	ASW_VADC_TH_L	[1:0]	ASW_VDAC_TH[1:0]	00	LSB - BITS OF 10 bit Adaptive control VDAC Threshold (0.78125mV/ LSB)
0x6F	ASW_BRI_TH_L	[7:0]	ASW_BRI_TH[7:0]	0000_0000	Adaptive control Brightness Threshold LSB (0.0061%/LSB)
0x70	ASW_BRI_TH_H	[5:0]	ASW_BRI_TH[13:8]	10_0000	Adaptive control Brightness Threshold MSB (0.0061%/LSB)

Function Descriptions (Cont.)

SPI Interface

For the data transfer a serial peripheral interface (SPI) is used. The SPI is configured to work only as SPI slave. If more than one driver is connected to a SPI master, they can be connected in a “Daisy Chain”-structure or a parallel structure.

SPI Daisy Chain Structure

All SPI slaves share the same clock (SCL) and chip select (xCS) signal. In that configuration all devices can be treated as one big shift register. The devices are automatically enumerated as described in the next section.
The APE5030A SDO pin was output 5V, when this pin want to use connection to micro controller then must noted to whether the MCU component can withstand 5V.
When SPI daisy chain structure is using series type then the device N SDO pin must choose the open drain type.

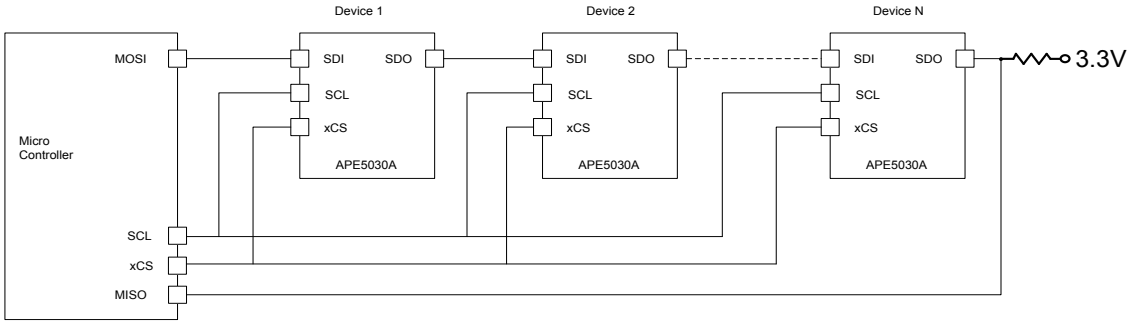


Figure 7: SPI Daisy Chain structure

SPI Parallel Structure

All SPI slaves share the same input (SDI) output (SDO) and clock (SCL) signal. Every single device can be addressed via the chip select (xCS) signal. In this configuration every device has the “DevAddr = 0x01”.
When SPI parallel structure was used then all device SDO pin must choose the open drain type.

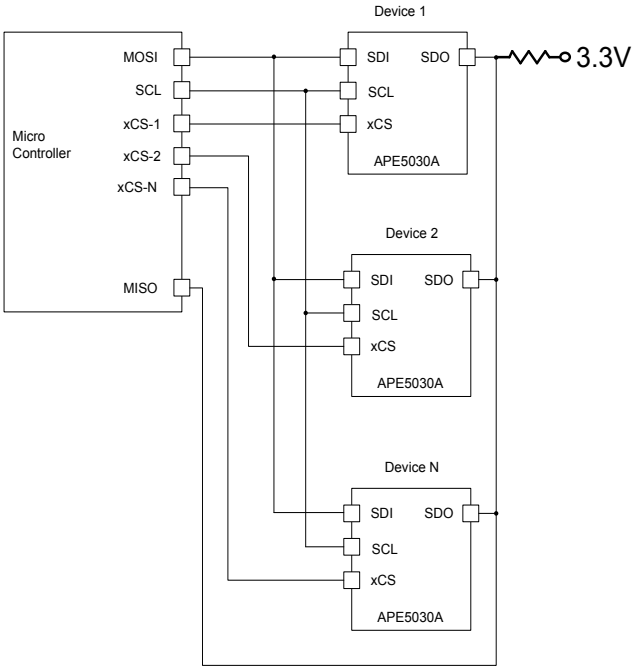


Figure 8: SPI Parallel Structure

Function Descriptions (Cont.)

SPI Device Address Enumeration

The device address of each driver is automatically set by the position of the device in the chain. The first device has DevAddr = 0x01, the second device has DevAddr = 0x02 and so on. Device Addresses 0x00 and 0x3F are used for special broadcast writing commands described below.

SPI Protocol Data Types

When xCS=0 all slaves will be activated. The addressing and data section is organized in byte packages. Each message can be built with the following Bytes:

B	S	Device Address [5:0]
Bit	Meaning	Description
B	Broadcast	B=1...Broadcast message to all devices (only WRITE) B=0...Normal message to one single device
S	Single byte	S=0...Block data read or write S=1...Single data transmission (only one byte)
Device Address [5:0]	Device Address	0x00 write/read same data to same register of all devices (B=1) 0x01 to 0x3E. Device addresses for device 1 to 62 0x3F Write different data to same register of all devices (B=1)

Nr_of_data

Defines the number of data bytes in the data frame if S=0

Nrofdata[7:0]		
Bit	Meaning	Description
Nrofdata[7:0]	Number of data bytes in frame	0x00 to 0xFF

Register_address

Register address to be read or written

R/W	Register Address [6:0]	
Bit	Meaning	Description
R/W	Read/Write	RW=0 write to register address RW=1 read from register address
Register Address[6:0]	Select register address	0x00 to 0x7F

Data

The data to be transferred

Data[7:0]		
Bit	Meaning	Description
Data[7:0]	Data	0x00 to 0xFF

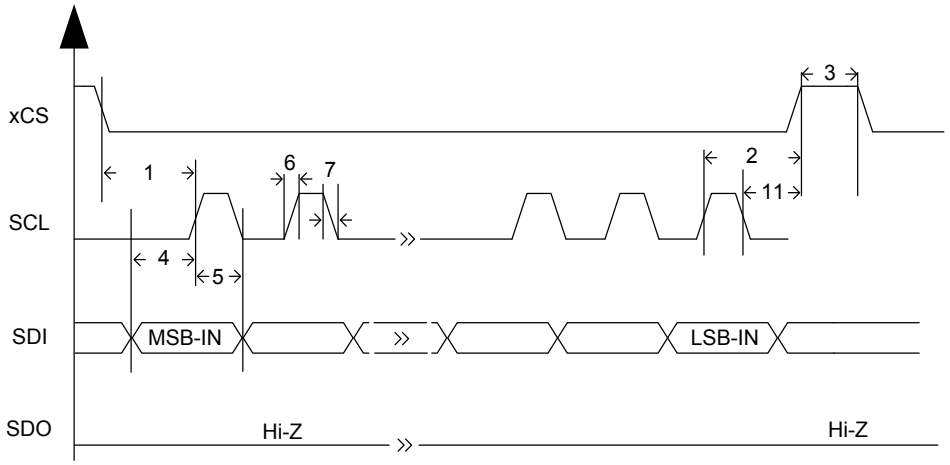
Function Descriptions (Cont.)

Time Characteristics

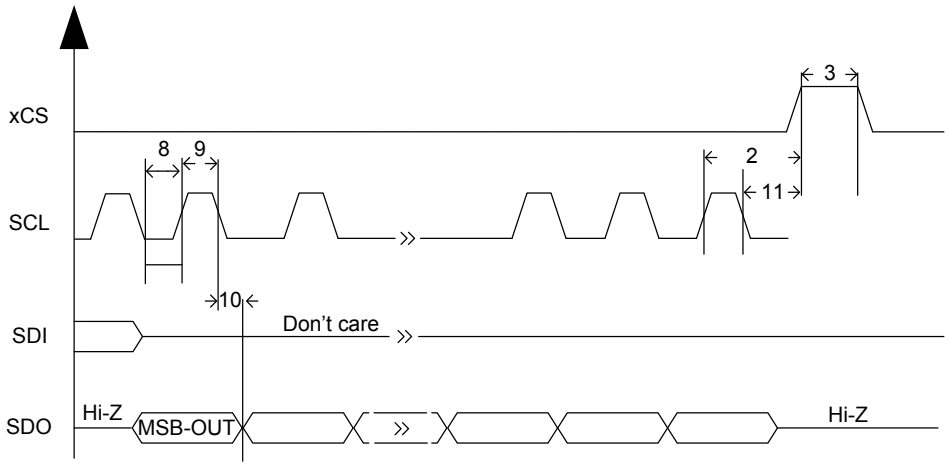
Symbol	Parameter	Min	Typ	Max	Unit
F_{CLK}	SCL frequency	0	-	10	MHz
t1	xCS setup time	50	-	-	ns
t2	xCS hold time	100	-	-	ns
t3	xCS disable time	100	-	-	ns
t4	SDI setup time	5	-	-	ns
t5	SDI hold time	5	-	-	ns
t6	SCL rise time	-	-	15	ns
t7	SCL falling time	-	-	15	ns
t8	SCL low time	40	-	-	ns
t9	SCL high time	40	-	-	ns
t10	Output valid from SCL low	-	-	11	ns
t11	SCL falling to xCS rising edge	50	-	-	ns

Timing Characteristics: Shows the timing characteristics of the SPI Interface

SPI Input Timing

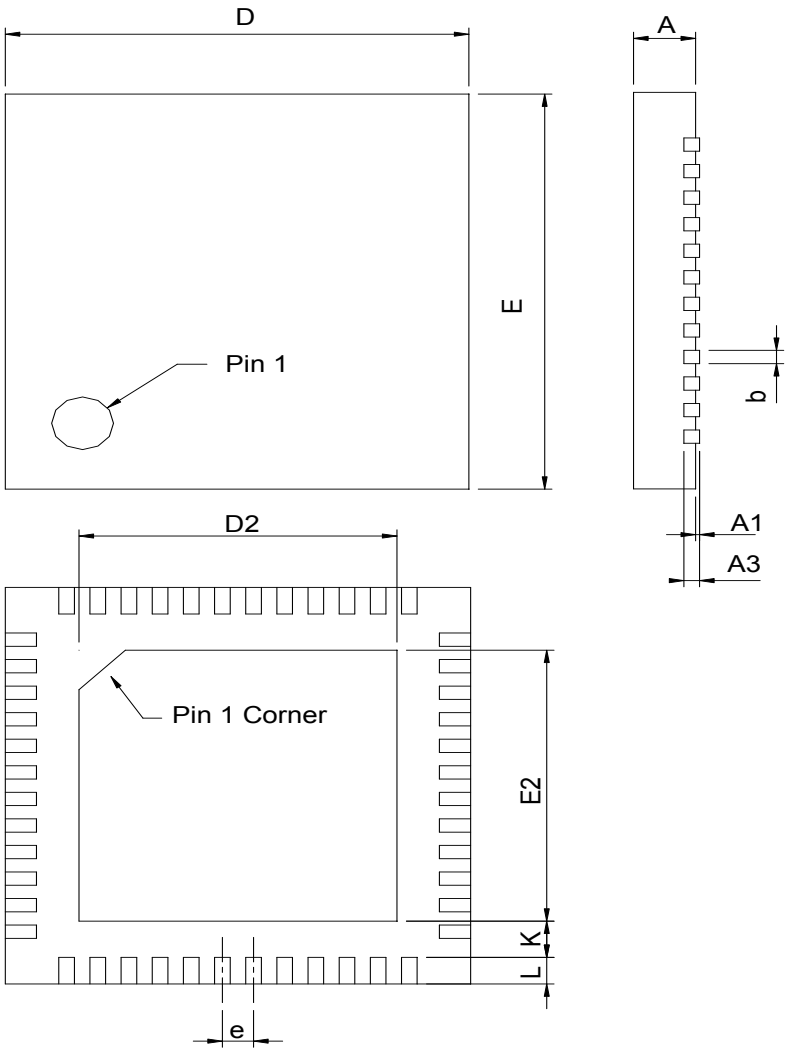


SPI Output Timing



Package Information

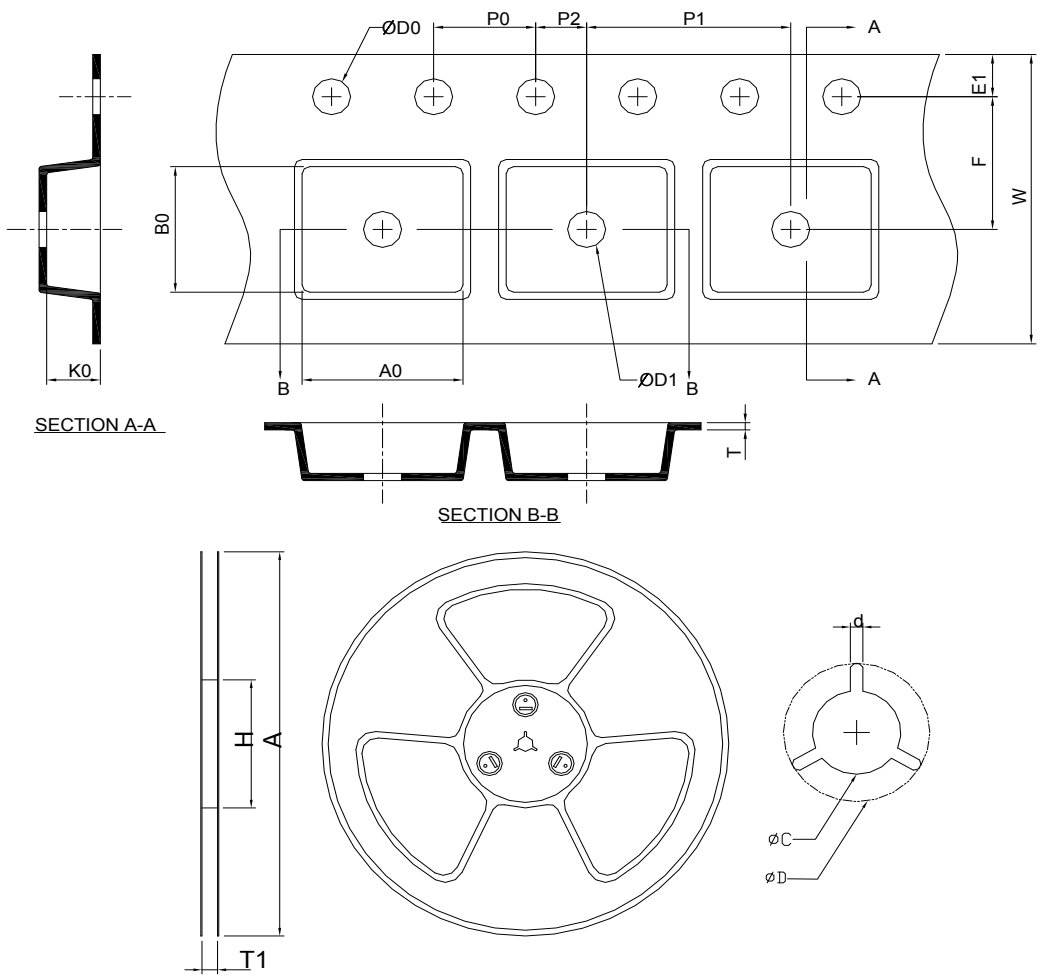
QFN7x7-48



SYMBOL	QFN7*7-48			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.90	7.10	0.272	0.280
D2	5.50	5.80	0.217	0.228
E	6.90	7.10	0.272	0.280
E2	5.50	5.80	0.217	0.228
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 WKKD-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN7x7-48	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	7.30±0.20	7.30±0.20	1.30±0.20

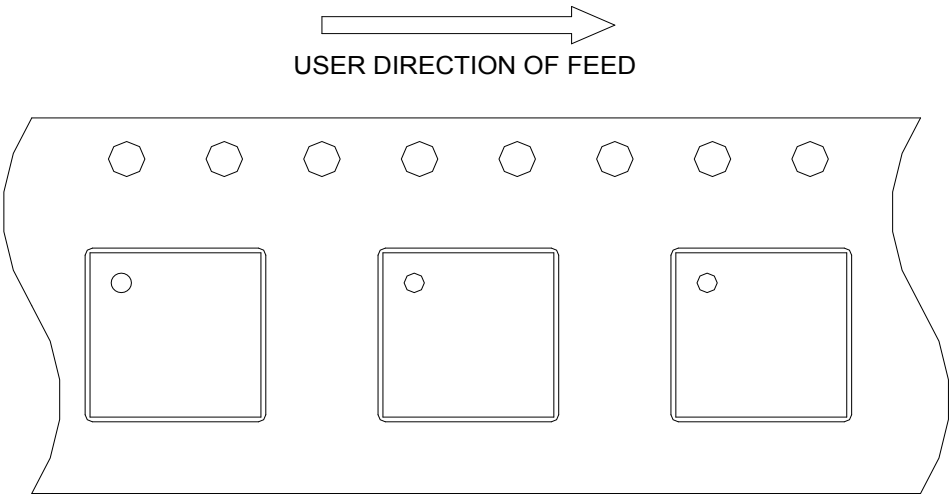
(mm)

Devices Per Unit

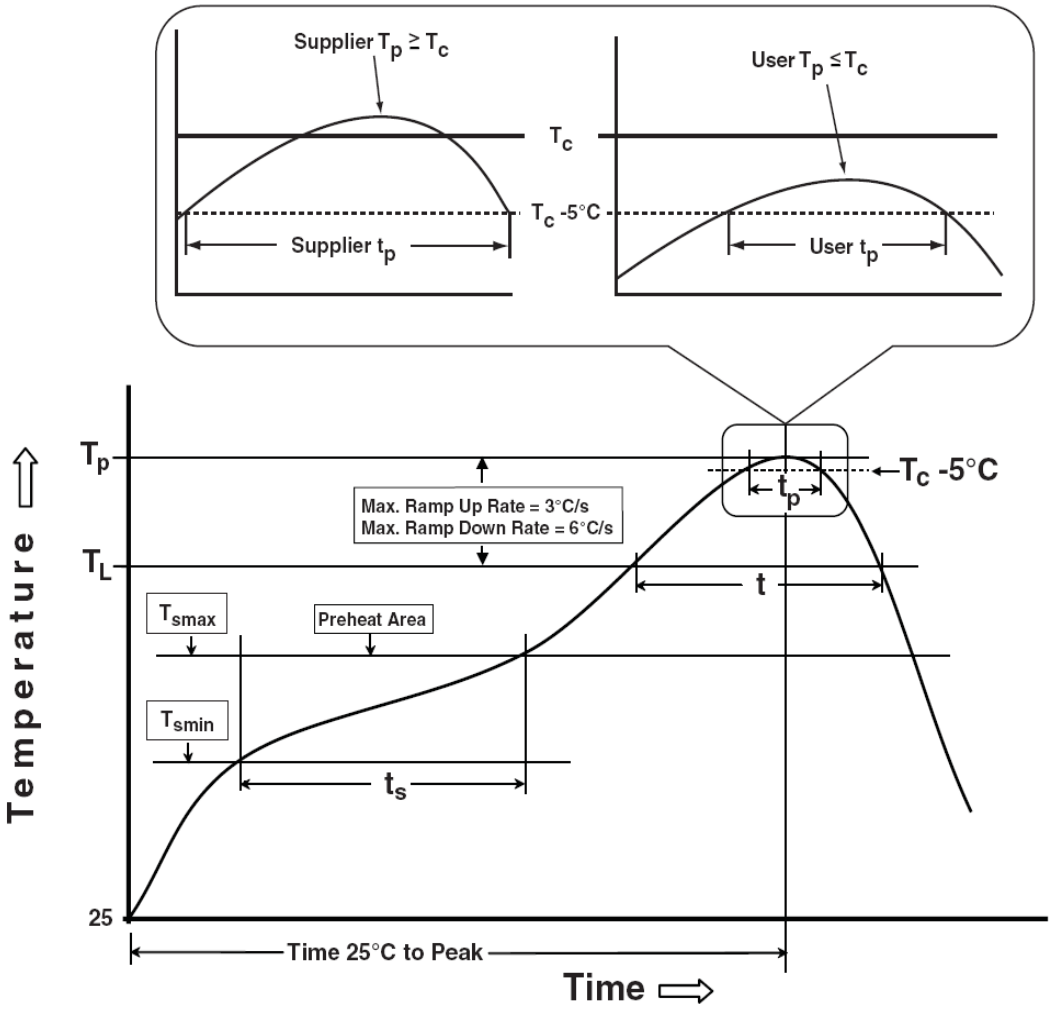
Package Type	Unit	Quantity
QFN7x7-48	Tape & Reel	2500

Taping Direction Information

QFN7x7-48



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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