Stereo 2.8W Audio Power Amplifier with DC Volume Control and Selectable Gain

Features

- **Operating Voltage : 4.5V to 5V**
- **Stereo Switchable Bridged/Single-Ended Power Amplifiers**
- **DC Volume Control Interface , 0dB to –78dB with Precision Scale**
- **Supply Current , I_{DD} = 15mA at Stereo BTL**
- **Low Shutdown Current , I_{DD} = 0.7μA**
- **Bridge-Tied Load (BTL) or Single-Ended-(SE) Modes Operation**
- **Output Power at 1% THD+N , V_{DD}=5V**
  - **–2.3W/Ch (typ) into a 3 Ω Load**
  - **–2.0W/Ch (typ) into a 4 Ω Load**
  - **–1.2W/Ch (typ) into a 8 Ω Load**
- **Output Power at 10% THD+N , V_{DD}=5V**
  - **–2.8W/Ch (typ) into a 3 Ω Load**
  - **–2.3W/Ch (typ) into a 4 Ω Load**
  - **–1.5W/Ch (typ) into a 8Ω Load**
- **Single-Ended Mode at 1.0% THD+N**
  - **–95mW/Ch (typ) into 32Ω Load**
- **Depop Circuitry Integrated**
- **Thermal Shutdown Protection and Over-Current Protection Circuitry**
- **High Supply Voltage Ripple Rejection**
- **PC99 Compliant**
- **28-pin TSSOP-P (with Enhanced Thermal Pad) Power Package Available**
- **Lead Free and Green Devices Available (RoHS Compliant)**

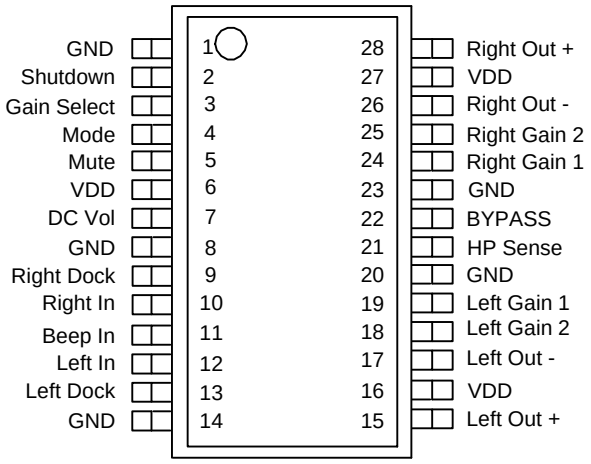
Applications

- **Notebook and Desktop Computers**
- **Multimedia Monitors**
- **Portable Applications**

General Description

The APA4838 is a monolithic integrated circuit, which provides DC volume control, and a stereo bridged audio power amplifiers capable of producing 2.8W (2.3W) into 3Ω with less than 10% (1.0%) THD+N. APA4838 includes a DC volume control, stereo bridge-tied and single-ended audio power amplifiers, stereo docking outputs, and a selectable gain control, that makes it optimally fittable for notebook PC, multimedia monitors, and other portable applications. The attenuator range of the volume control in APA4838 is from 0dB (DC_Vol=0.8V_{DD}) to –78dB (DC_Vol=0V) with 31 steps. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA4838, that reduces pops and clicks noise during power up or shutdown mode operation, and protects the chip from being destroyed by over temperature failure. To simplify the audio system design, APA4838 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the HP Sense input control pin signal. Besides the low supply current design to increase the efficiency of the amplifiers, APA4838 also features a shutdown function which keeps the supply current only 0.7μA (typ).

Pin Configuration



Ordering and Marking Information

APA4838 □□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code R : TSSOP-28P Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APA4838 R : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN}	Input Voltage Range, HP sense, Shutdown, Mute, Mode, Gain Select	-0.3 to V_{DD}+0.3	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	Internally Limited	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Maximum Lead Soldering Temperature, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note 1 :APA4838 integrated internal thermal shutdown protection when junction temperature ramp up to 150°C

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air (Note 2) TSSOP-28P	45	°C/W

Note 2 : 5 in^2 printed circuit board with 2oz trace and copper pad through 9 25mil diameter vias. The thermal pad on the TSSOP_P package with solder on the printed circuit board.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		4.5 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	Shutdown, Mute, Mode, Gain Select	2 ~	V
		HP Sense	4 ~	V
V_{IL}	Low Level Threshold Voltage	Shutdown, Mute, Mode, Gain Select	~ 1.0	V
		HP Sense	~ 3	V
V_{ICM}	Common Mode Input Voltage		V_{DD}-1.0 ~	V

Electrical Characteristics

Electrical Characteristics for Entire IC

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T_A= 25°C

Symbol	Parameter	Test Conditions	APA4838			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		4.5	-	5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V, I_O=0A	-	15	25	mA
I_{SD}	Shutdown Current	$V_{PIN\ 2}$= V_{DD}	-	0.7	2.0	µA

Electrical Characteristics for Volume Attenuators

The following specifications apply for V_{DD}= 5V. Limits apply for T_A= 25°C

Symbol	Parameter	Test Conditions	APA4838			Unit
			Min.	Typ.	Max.	
C_{RANGE}	Attenuator Range	Gain with $V_{PIN\ 7}$=5V	-	-	±0.5	dB
		Attenuation with $V_{PIN\ 7}$=0V	-65	-78	-	
A_M	Mute Attenuation	$V_{PIN\ 5}$=5V, Bridged Mode	-70	-	-	dB
		$V_{PIN\ 5}$=5V, Single-Ended Mode	-70	-	-	

Electrical Characteristics for BTL Mode Operation

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T_A= 25°C

Symbol	Parameter	Test Conditions	APA4838			Unit
			Min.	Typ.	Max.	
V_{OS}	Output Offset Voltage	V_{IN}=0V	-	5	-	mV
P_O	Output Power	THD+N=1%, f_{in}=1kHz R_L=3Ω R_L=4Ω R_L=8Ω THD+N=10%, f_{in}=1kHz R_L=8Ω	- -	2.3 2.0 1.2 1.5	- -	W
THD+N	Total Harmonic Distortion + Noise	A_{VD}=2, f_{in}=1kHz R_L=4Ω, P_O =1.5W R_L=8Ω, P_O=1W	-	0.07 0.07		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=100mV_{Rms} C_B=2.2µF, R_L=8Ω, f_{in}=1kHz	-	70	-	dB
Crosstalk	Channel Separation	C_B=2.2µF, f_{in}=1kHz, R_L=8Ω	-	90	-	dB
S/N	Signal-to-Noise Ratio	V_{DD}=5V, P_O =1.1W, R_L=8Ω,A-Weighting Filter	-	95	-	dB
V_N	Output Noise Voltage	R_L=8Ω,A-Weighting Filter	-	30	-	µV

Electrical Characteristics (Cont.)

Electrical Characteristics for BTL Mode Operation

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T_A= 25°C

Symbol	Parameter	Test Conditions	APA4838			Unit
			Min.	Typ.	Max.	
V_{OS}	Output Offset Voltage	V_{IN}=0V	-	5	-	mV
P_O	Output Power	THD+N=1%, f_{in}=1kHz R_L=3Ω R_L=4Ω R_L=8Ω THD+N=10%, f_{in}=1kHz R_L=8Ω	- -	 2.3 2.0 1.2 1.5	- -	W
THD+N	Total Harmonic Distortion + Noise	A_{VD}=2, f_{in}=1kHz R_L=4Ω , P_O =1.5W R_L=8Ω , P_O=1W	-	 0.07 0.07	-	%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=100mV_{Rms} C_B=2.2µF, R_L=8Ω, f_{in}=1kHz	-	70	-	dB
Crosstalk	Channel Separation	C_B=2.2µF, f_{in}=1kHz, R_L=8Ω	-	90	-	dB
S/N	Signal-to-Noise Ratio	V_{DD}=5V, P_O =1.1W, R_L=8Ω,A-Weighting Filter	-	95	-	dB
V_N	Output Noise Voltage	R_L=8Ω,A-Weighting Filter	-	30	-	µV

Electrical Characteristics for SE Mode Operation

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T_A= 25°C

Symbol	Parameter	Test Conditions	APA4838			Unit
			Min.	Typ.	Max.	
V_{OS}	Output Offset Voltage	V_{IN}=0V	-	5	-	mV
P_O	Output Power	THD+N=1%, f_{in}=1kHz	-	95	-	mW
		THD+N=10%, f_{in}=1kHz	-	110	-	
THD+N	Total Harmonic Distortion Plus Noise	A_V= 1, V_{OUT}=1V_{RMS}, R_L=10kΩ, f_{in}=1kHz	-	0.05	-	%
		P_O =75mW, R_L=32Ω, A_V= 1, f_{in}=1kHz	-	0.07	-	%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=100mV_{RMS}, f_{in}=120Hz, C_B=2.2µF	-	52		dB
Crosstalk	Channel Separation	C_B=2.2µF, R_L=8Ω , f_{in}=1kHz	-	90	-	dB
S/N	Signal-to-Noise Ratio	P_O =75mW, R_L=32Ω, A-Weighting Filter	-	102	-	dB
V_N	Output Noise Voltage	R_L=32Ω, A-Weighting Filter	-	20	-	µV

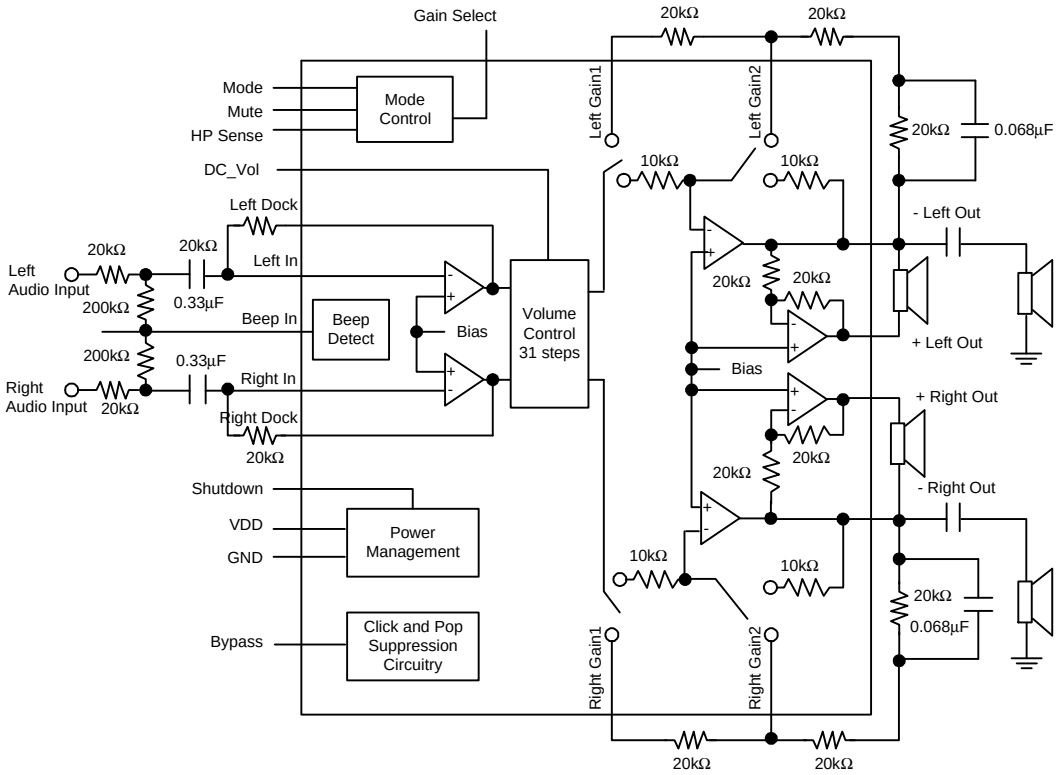
Pin Description

PIN		I/O	FUNCTION
NAME	NO.		
GND	1, 8, 14, 20, 23		Ground connection for circuitry.
Shutdown	2	I	Shutdown mode control signal input, place entire IC in shutdown mode when held high, Idd=0.7μA
Gain Select	3	I	Gain select input pin, logic high will switch the amplifier to external gain mode, and logic low will switch to internal unity gain.
Mode	4	I	Mode select input pin, fixed gain when logic L and gain adjustable mode when logic H.
Mute	5	I	Mute control input pin, active H.
VDD	6, 16, 27		Supply voltage input pin
DC_Vol	7	I	Volume control function input pin.
Right Dock	9	O	Right docking output pin
Right In	10	I	Right channel audio input pin
Beep In	11	I	Beep signal input pin
Left In	12	I	Left channel audio input pin
Left Dock	13	O	Right docking output pin
Left Out +	15	O	Left channel positive output pin
Left Out -	17	O	Left channel negative output pin
Left Gain 2	18		Connect pin 2 of the external gain setting resistor for left channel
Left Gain 1	19		Connect pin 1 of the external gain setting resistor for left channel
HP Sense	21	I	Headphone sense control pin
Bypass	22		Bypass pin
Right Gain 1	24		Connect pin 1 of the external gain setting resistor for right channel
Right Gain 2	25		Connect pin 2 of the external gain setting resistor for right channel
Right Out -	26	O	Right channel negative output pin
Right Out +	28	O	Right channel positive output pin

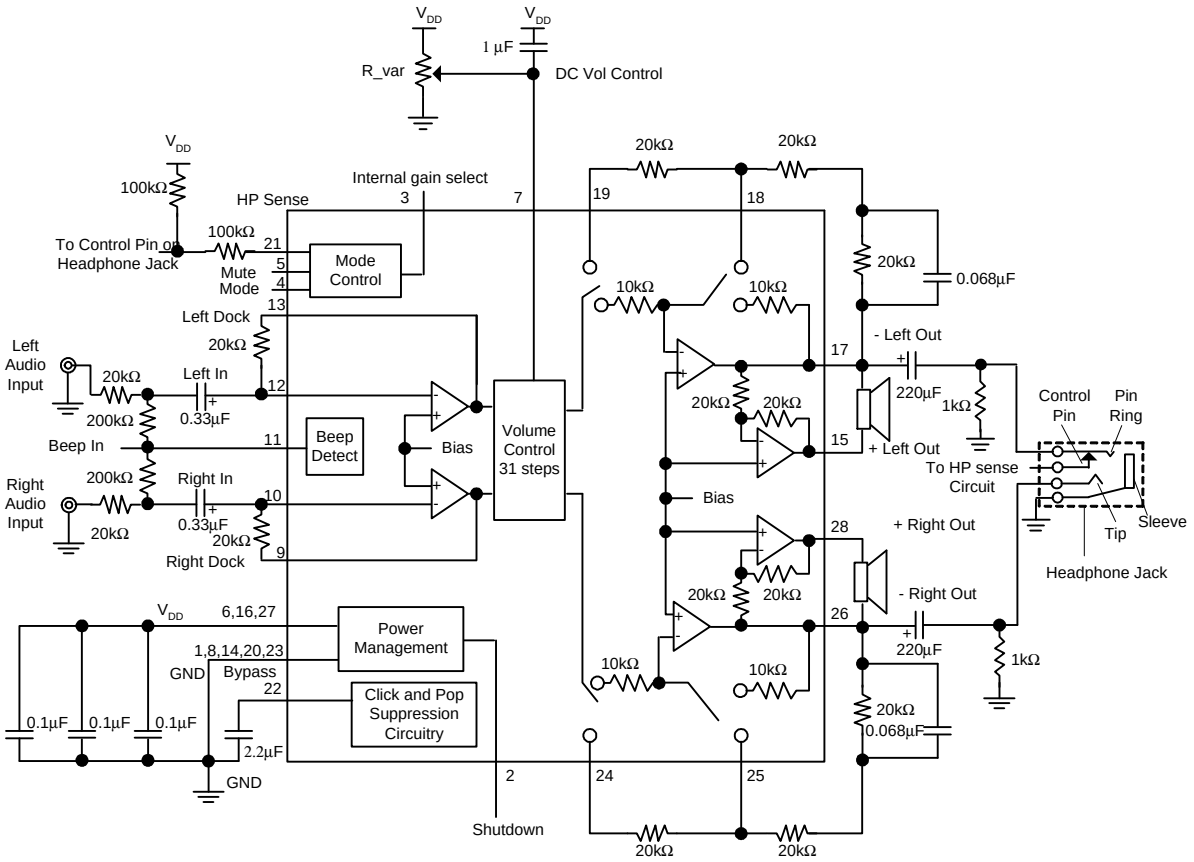
Truth Table for Logic Inputs

Mute	Gain Select	Mode	HP Sense	Gain Mode of Power Amplifier	DC Vol. Control	BTL Output	SE Output
0	0	0	0	Unity Gain Setting	Fixed Level	Vol. Fixed	-
0	0	0	1	Unity Gain Setting	Fixed Level	Muted	Vol. Fixed
0	0	1	0	Unity Gain Setting	Adjustable	Vol. Adjustable	-
0	0	1	1	Unity Gain Setting	Adjustable	Muted	Vol. Adjustable
0	1	0	0	External Gain Setting	Fixed Level	Vol. Fixed	-
0	1	0	1	External Gain Setting	Fixed Level	Muted	Vol. Fixed
0	1	1	0	External Gain Setting	Adjustable	Vol. Adjustable	-
0	1	1	1	External Gain Setting	Adjustable	Muted	Vol. Adjustable
1	X	X	X	-	-	Muted	Muted

Block Diagram



Typical Application Circuit



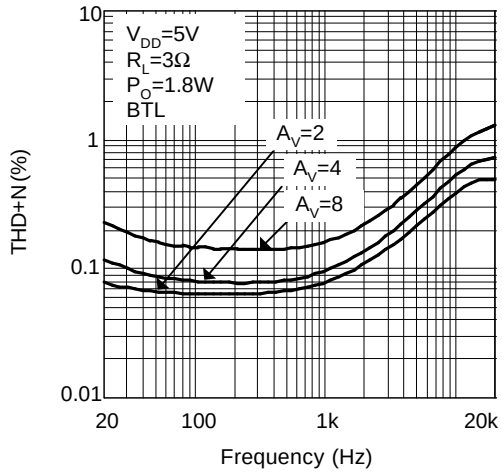
Application Information

Volume Control Table

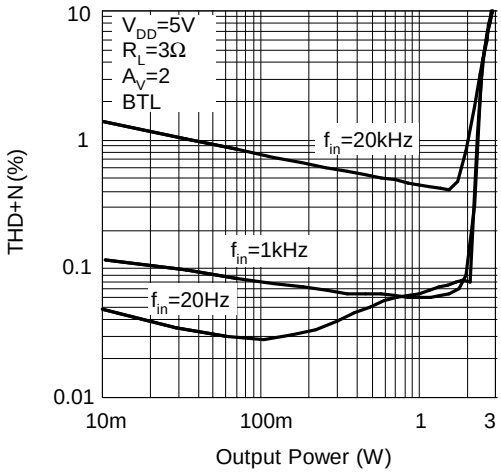
Gain (dB)	Voltage Range (% of V_{DD})			Voltage Range (V_{DD}=5V)		
	Low	High	Recommended	Low	High	Recommended
0	77.5%	100.00%	100.000%	3.875	5.000	5.000
-1	75.0%	78.5%	76.875%	3.750	3.938	3.844
-2	72.5%	76.25%	74.375%	3.625	3.813	3.719
-3	70.0%	73.75%	71.875%	3.500	3.688	3.594
-4	67.5%	71.25%	69.375%	3.375	3.563	3.469
-5	65.0%	68.75%	66.875%	3.250	3.438	3.344
-6	62.5%	66.25%	64.375%	3.125	3.313	3.219
-8	60.0%	63.75%	61.875%	3.000	3.188	3.094
-10	57.5%	61.25%	59.375%	2.875	3.063	2.969
-12	55.0%	58.75%	56.875%	2.750	2.938	2.844
-14	52.5%	56.25%	54.375%	2.625	2.813	2.719
-16	50.0%	53.75%	51.875%	2.500	2.688	2.594
-18	47.5%	51.25%	49.375%	2.375	2.563	2.469
-20	45.0%	48.75%	46.875%	2.250	2.438	2.344
-22	42.5%	46.25%	44.375%	2.125	2.313	2.219
-24	40.0%	43.75%	41.875%	2.000	2.188	2.094
-26	37.5%	41.25%	39.375%	1.875	2.063	1.969
-28	35.0%	38.75%	36.875%	1.750	1.938	1.844
-30	32.5%	36.25%	34.375%	1.625	1.813	1.719
-32	30.0%	33.75%	31.875%	1.500	1.688	1.594
-34	27.5%	31.25%	29.375%	1.375	1.563	1.469
-36	25.0%	28.75%	26.875%	1.250	1.438	1.344
-38	22.5%	26.25%	24.675%	1.125	1.313	1.219
-40	20.0%	23.75%	21.875%	1.000	1.188	1.094
-42	17.5%	21.25%	19.375%	0.875	1.063	0.969
-44	15.0%	18.75%	16.875%	0.750	0.937	0.844
-46	12.5%	16.25%	14.375%	0.625	0.812	0.719
-48	10.0%	13.75%	11.875%	0.500	0.687	0.594
-50	7.5%	11.25%	9.375%	0.375	0.562	0.469
-52	5.0%	8.75%	6.875%	0.250	0.437	0.344
-78	0.0%	6.25%	0.000%	0.000	0.312	0.000

Typical Operating Characteristics

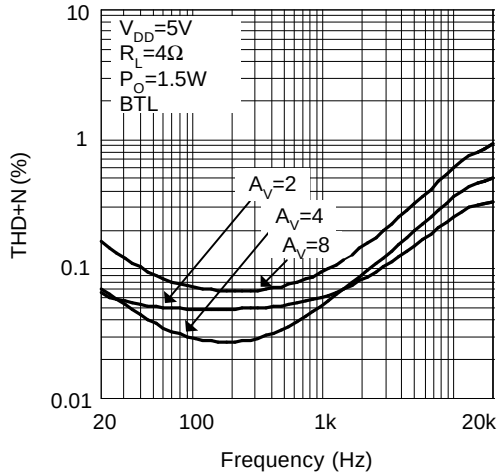
THD+N vs. Frequency



THD+N vs. Output Power



THD+N vs. Frequency



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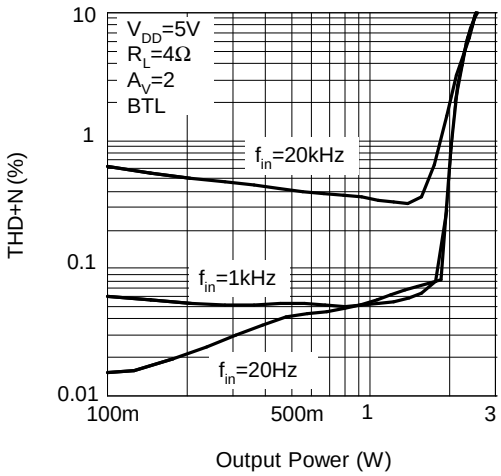
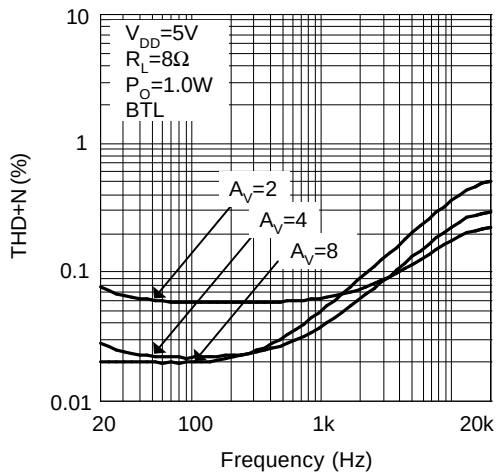
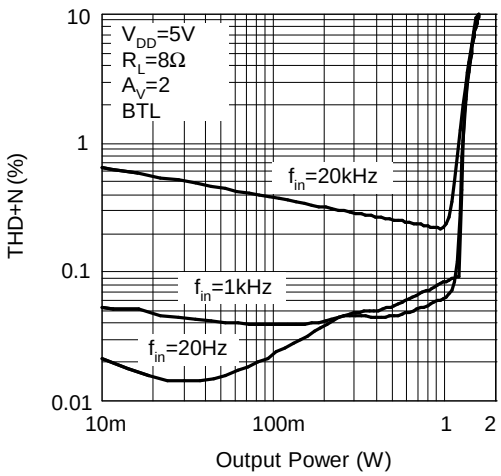


THD+N vs. Frequency

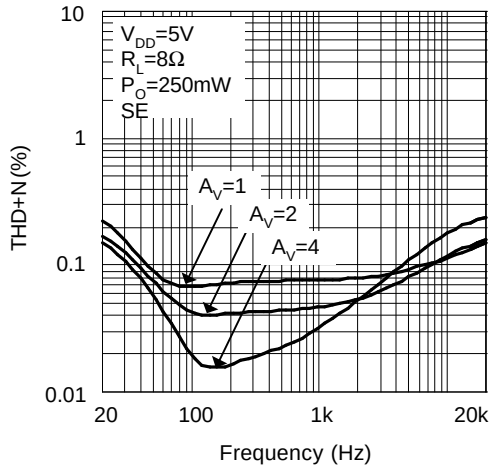


THD+N vs. Output Power

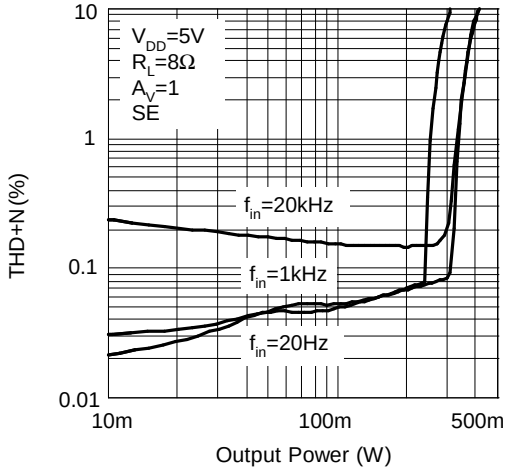


Typical Operating Characteristics (Cont.)

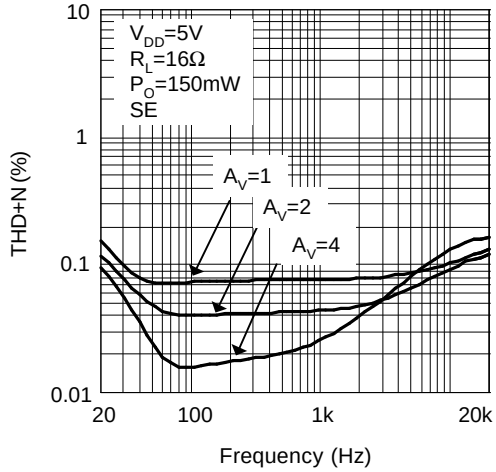
THD+N vs. Frequency



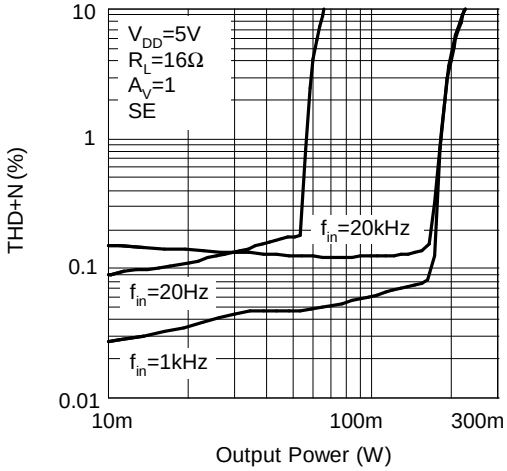
THD+N vs. Output Power



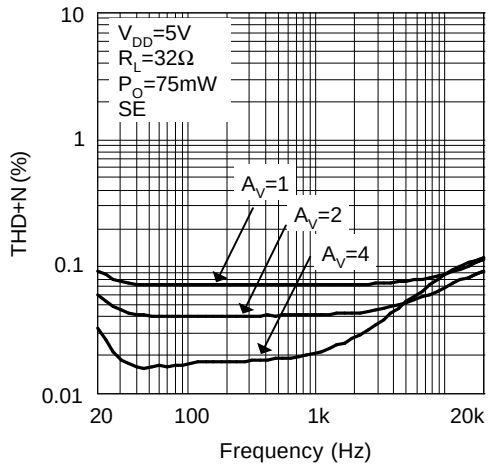
THD+N vs. Frequency



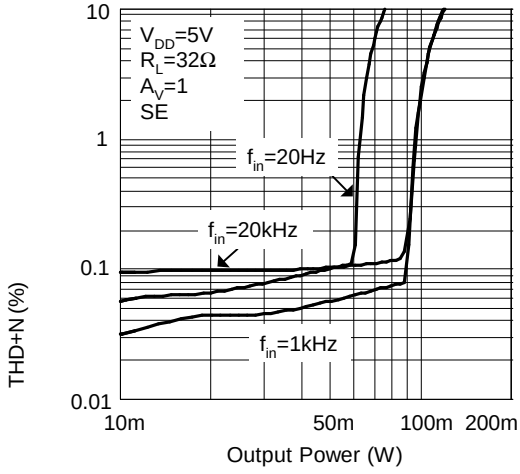
THD+N vs. Output Power



THD+N vs. Frequency

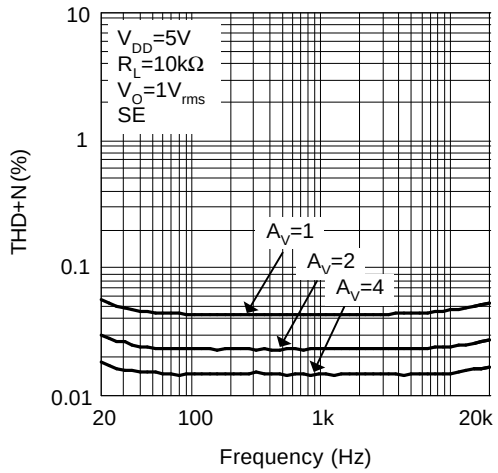


THD+N vs. Output Power

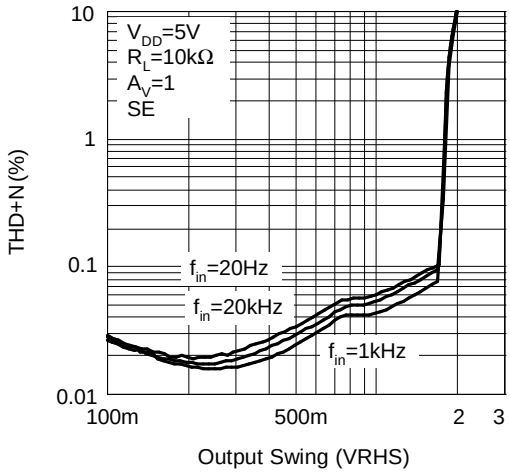


Typical OperatingCharacteristics (Cont.)

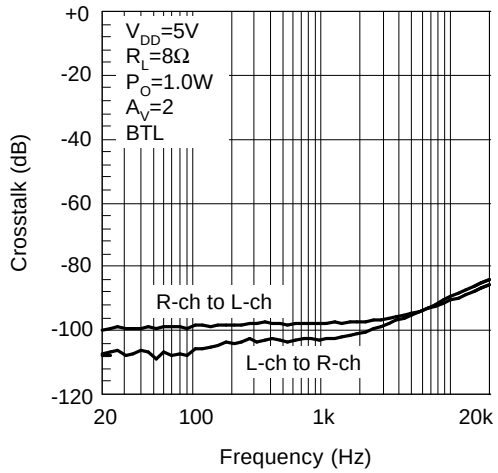
THD+N vs. Frequency



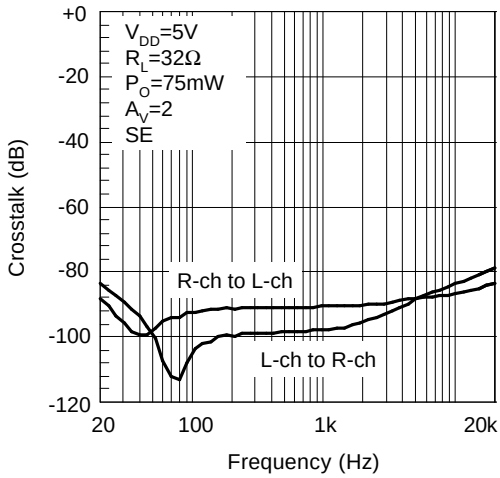
THD+N vs. Output Swing



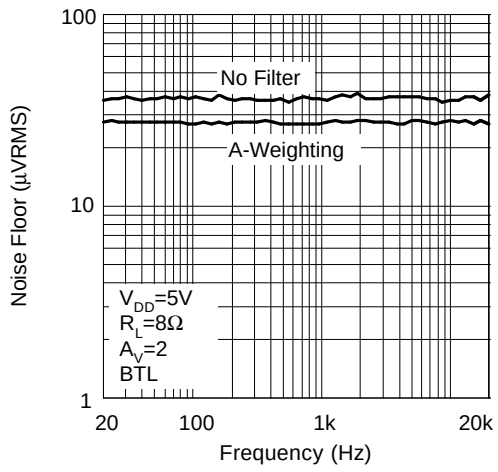
Crosstalk vs. Frequency



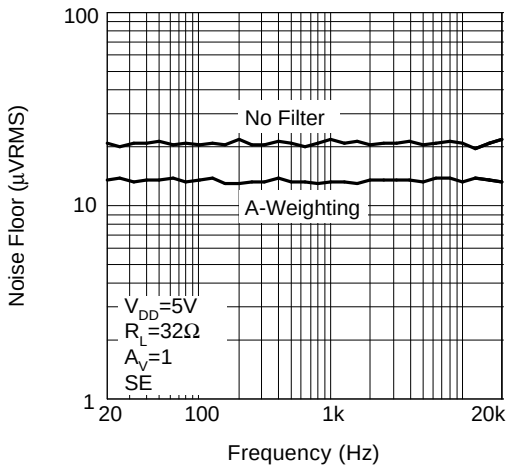
Crosstalk vs. Frequency



Noise Floor vs. Frequency

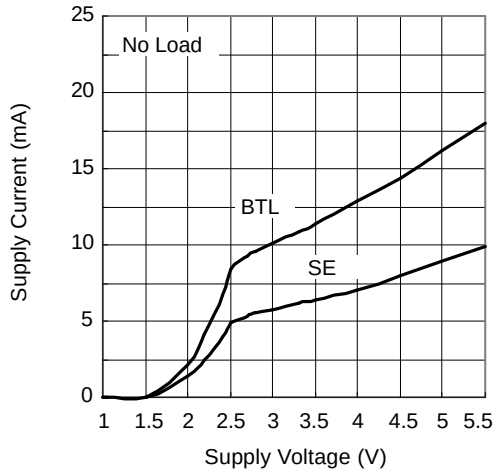


Noise Floor vs. Frequency

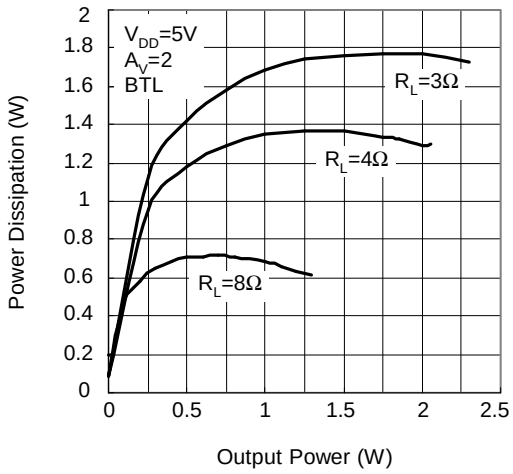


Typical Operating Characteristics (Cont.)

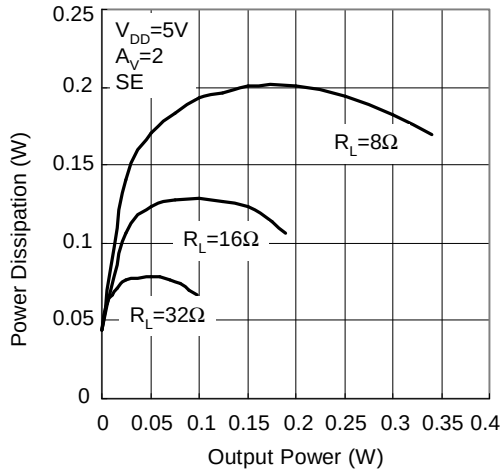
Supply Current vs. Supply Voltage



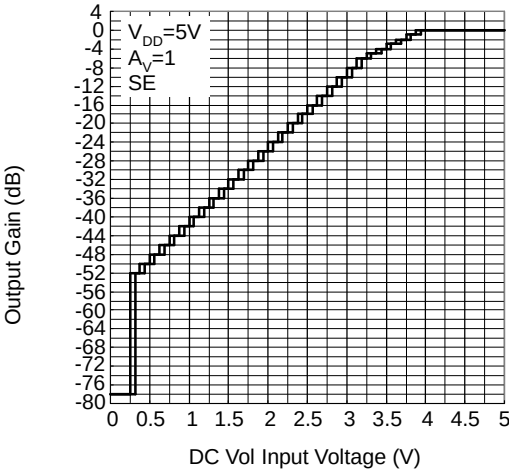
Power Dissipation vs. Output Power



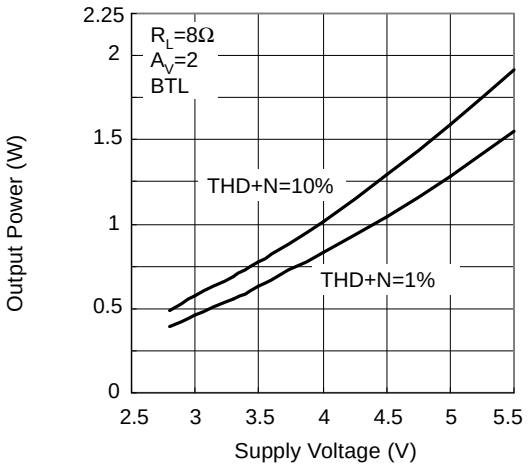
Power Dissipation vs. Output Power



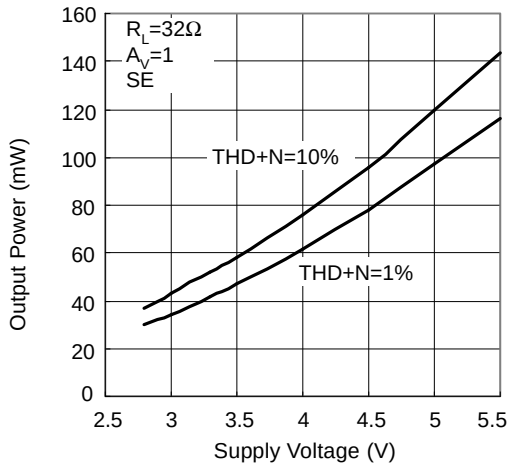
Gain vs. Voltage, 5V, SE



Output Power vs. Supply Voltage

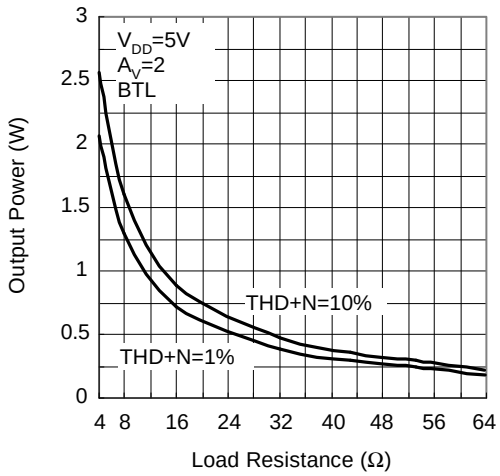


Output Power vs. Supply Voltage

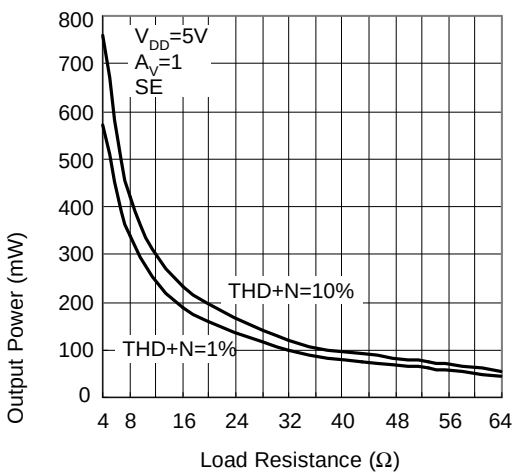


Typical Operating Characteristics (Cont.)

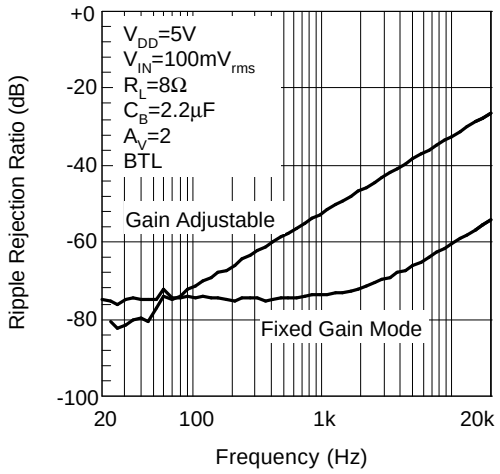
Output Power vs. Load Resistance



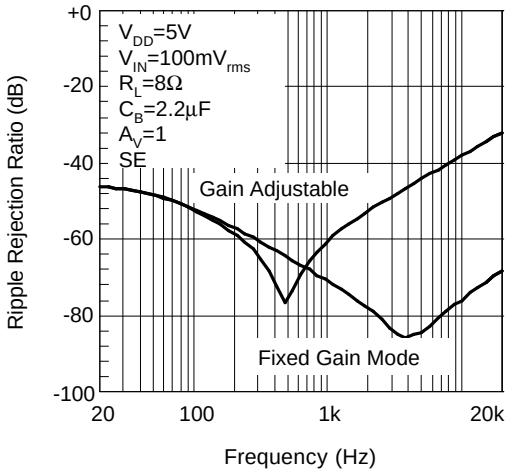
Output Power vs. Load Resistance



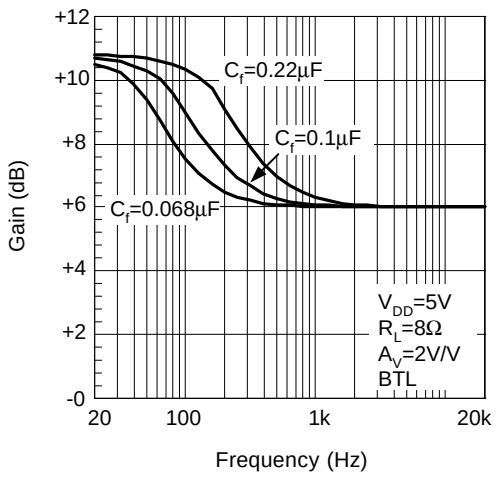
PSRR vs. Frequency



PSRR vs. Frequency



Gain vs. Frequency



Application Information

BTL Operation

The APA4838 output stage (power amplifier) has two pairs of operational amplifiers internally, allowed for different amplifier configurations for each channel.

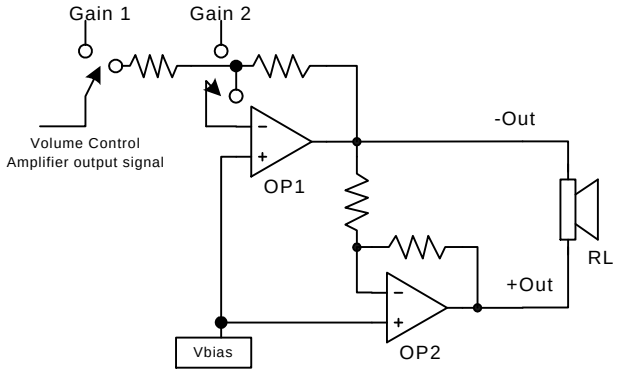


Figure 1: APA4838 Power Amplifier Internal Configuration (each channel)

The power amplifier OP1 gain is set by internal unity-gain or external gain setting which is selected from Gain Select pin and the audio input signal come from internal volume control block while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of both amplifiers with identical in magnitude but out of phase 180°. Consequently, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs -Out and +Out, an amplifier configuration commonly referred to bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to the ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage.

When placed under the same conditions, a BTL amplifier has four times the output power of a SE amplifier. A BTL configuration, such as the one used in APA4838, also creates a second advantage over SE amplifiers. Since the differential outputs, +Right Out, -Right Out, +Left Out, and -Left Out, are biased at half-supply, it is not necessary for DC voltage to be across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF), so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).

The rules described still hold with the addition of the following relationship:

$$\frac{1}{C_B \times 125k\Omega} \leq \frac{1}{R_I C_I} << \frac{1}{R_L C_C} \qquad (1)$$

Output SE/$\overline{\text{BTL}}$ Operation

The best cost saving feature of APA4838 is that it can be switched easily between BTL and SE modes. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the APA4838, two separate amplifiers drive –Out and +Out for each channel (See Figure 1). The HP Sense input controls the operation of the follower amplifier that drives +Left Out and +Right Out.

- When HP Sense is held low, the OP2 is turn on and the APA4838 is in the BTL mode.
- When HP Sense is held high, the OP2 is in a high output impedance state, which configures the APA4838 as SE driver from -Out. I_{DD} is reduced by approximately one-half in SE mode.

The control of the HP Sense input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in the Application Circuit.

Application Information (Cont.)

Output SE/$\overline{BTL}$ Operation (Cont.)

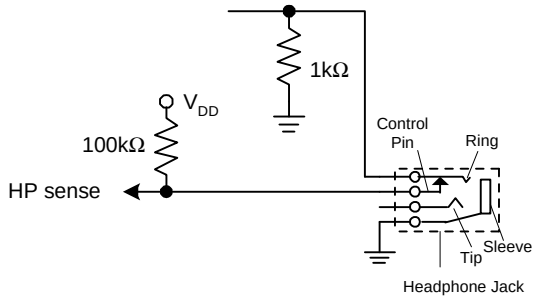


Figure 2: HP Sense Input Selection by Phonejack plug

In Figure 2, input HP Sense operates as below:
When the phonejack plug is inserted, the 1kΩ resistor is disconnected and the HP Sense input is pulled high and enables the SE mode.
When this input goes to a high level, the +Out amplifier is shutdown which causes the speaker to mute. The -Out amplifier then drives through the output capacitor (C_O) into the headphone jack.
When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the HP Sense pin, enabling the BTL function.

Docking Output Signal

APA4835 internal first amplifier is used as audio signal pre-amplfier and feedback resistor is connected between Dock output pin and audio input pin. However, the internal first amplifier's closed-loop gain can be adjusted using external resistors. Use Equation 2 to determine the input and feedback resistor values for a desired gain.

$$A_V = -\frac{R_f}{R_i} \quad (2)$$

The Dock output signal provides low distortion audio quality for light driving output. ex. active speaker, monitors or audio/visual equipment. These two outputs can driving load of >1kΩ with rail-to-rail output and output coupling capacitor is required when using these outputs.
Typical values for the output coupling capacitors are 0.33µF to 1.0µF. If polarized coupling capacitors are used, connect their '+' terminals to the respective output pin.

The Right Dock and Left Dock channel outputs signal are also used to drive internal volume control amplifier.

Input Capacitor, C_i

In the typical application an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the following equation:

$$f_C(\text{highpass}) = \frac{1}{2\pi R_i C_i} \quad (3)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 100kΩ and the specification calls for a flat bass response down to 40Hz. Equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_C} \quad (4)$$

When the input resistance variation is considered, the C_i is 0.04µF, therefore, a value in the range of 0.1µF to 1.0µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i+R_f, C_i) to the load.
This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' input in most applications because the DC level of the amplifiers' inputs are held at V_{DD}/2. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

As to the other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.
The capacitors located on the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor will improve PSRR due to increased half-supply stability. Typical ap-

Application Information (Cont.)

Effective Bypass Capacitor, C_B (Cont.)

plication employ a 5V regulator with 1.0µF and a 0.1µF bypass as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA4838. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid the start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (5) should be maintained.

$$\frac{1}{C_B \times 125k\Omega} << \frac{1}{R_i C_i} \quad (5)$$

The bypass capacitor is fed from a 125kΩ resistor inside the amplifier. Bypass capacitor, C_B, values of 3.3µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effects to the start-up time. It is determined in the following equation:

$$Tstart\ up = 5 \times (C_B \times 125k\Omega) \quad (6)$$

Output Coupling Capacitor, C_O

In the typical single-supply (SE) configuration, an output coupling capacitor (C_O) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the following equation:

$$f_C(highpass) = \frac{1}{2\pi R_L C_O} \quad (7)$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main performance disadvantage is that the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_O are required to pass low frequencies into the load.

Power Supply Decoupling, C_S

The APA4838 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA4838 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry. The value of C_i will also affect turn-on pops.(Refer to Effective Bypass Capacitance) The bypass voltage should rise slower than input bias voltage.

Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time.

In a SE configuration, the output coupling capacitor, C_O, is of particular concern. This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_O, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current.

In most cases, choosing a small value of Ci in the range of 0.33µF to 1µF, C_B being equal to 4.7µF and an external 1kΩ resistor should be placed in parallel with the internal

Application Information (Cont.)

Optimizing Depop Circuitry (Cont.)

10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Therefore, it is advantageous to use low-gain configurations.

Shutdown and Mute Function

In order to reduce power consumption while not in use, the APA4838 contains a Shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the Shutdown pin.

The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between the ground and the supply voltage V_{DD} to provide maximum device performance.

By switching the Shutdown pin to high level, the amplifier enters a low-current state, I_{DD}<1μA. APA4838 is in shutdown mode. On normal operating, Shutdown pin pulls to low level to keeping the IC out of the shutdown mode. The Shutdown pin should be tied to a definite voltage to avoid unwanted state changing.

The APA4838 mutes the amplifier and DOCK outputs when V_{DD} is applied to the Mute pin. Even while muted, the APA4838 will amplify a system alert (beep) signal whose magnitude satisfies the PCBEEP detect circuitry. Applying 0V to the Mute pin returns the APA4838 to normal operation. Prevent unanticipated mute behavior by connecting the Mute pin to V_{DD} or ground. Do not let the Mute pin float.

PCBEEP Detect Circuitry

APA4838 integrates a PCBEEP detect circuit for notebook and computer used. When Beep In signal is greater than 1/2V_{DD}, the PCBEEP mode is active. APA4838 will force to BTL mode and the internal fixed gain mode. The Beep In signal becomes the amplifier input signal and plays on the system speaker without coupling capacitor. Use input resistor between stereo input pin and Beep In to attenuate Beep In signal. These resistors are shown as 200kΩ devices in Application Circuit. Use higher value resistors to reduce the gain applied to the beep signal.

If the amplifier in the mute mode, it will out of mute mode whenever PCBEEP mode enable. The APA4838's shutdown mode must be deactivated before a system alert signal is applied to Beep In pin. The APA4838 will return to previous setting when it is out of PCBEEP mode. The Beep In pin should be tied to a ground when not used to avoid unwanted state changing.

Mode Function

The APA4838's Mode function has 2 states controlled by the voltage applied to the Mode pin. By applying 0V to the Mode pin, forces the APA4838 to fixed gain amplifier and internal volume control block will be disable and internal first amplifier output signal (Dock) to power amplifier directly. When Mode pin goes to high level, which uses the internal DC controlled volume control is selected. This mode sets the amplifier's gain according to the DC voltage applied to the DC Vol control pin. Do not let the Mode pin float when it does not be used.

Internal and External Gain Selection

APA4838 provides external gain setting for base boost function or internal feedback gain setting which is decided by Gain Select control input. If Gain Select pin goes high level, the gain setting will be defined by Gain1 and Gain2 pin. When Gain Select pin tied to low level, APA4835 power amplifier gain setting as unit gain by internal resistor.

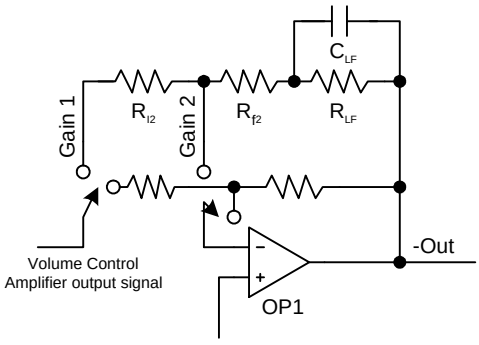


Figure3: Bass Boost Gain Setting Configuration

In some cases, a designer may want to improve the low frequency response of the bridged amplifier or incorporate a bass boost feature. Refer to the Figure 3, a resistor,

Application Information (Cont.)

Internal and External Gain Selection (Cont.)

R_{LF}, and a capacitor, C_{LF}, in parallel, can be placed in series with the feedback resistor of the bridged amplifier as seen in Figure 3.

$$f_c = \frac{1}{2\pi R_{LF} C_{LF}} \quad (8)$$

The bridged-amplifier low frequency differential gain is:

$$f_c = \frac{2x(R_{i2}+R_{LF})}{R_{i2}} \quad (9)$$

Using the component values shown in Figure 3 (R_{F2} = 20kΩ,R_{LF} = 20kΩ, and C_{LF} = 0.068μF), a first-order, -6dB pole is created at 120Hz. Assuming R_{i2} = 20kΩ, the low frequency differential gain is 4. The input (C_I) and output (C_O) capacitor values must be selected for a low frequency response that covers the range of frequencies affected by the desired bass-boost operation.

At low frequencies, C_{LF} is a virtual open circuit and at high frequencies, its nearly zero ohm impedance shorts R_{LF}. The result is increased bridge-amplifier gain at low frequencies. The combination of R_{LF} and C_{LF} form a -6dB corner frequency at 120Hz.

Volume Adjustable and Fixed Gain selection

The APA4838 has an internal stereo volume control whose setting is the function of the DC voltage applied to the DC Vol control pin. The APA4838 volume control consists of 31 steps that are individually selected by a variable DC voltage level on the DC Vol control pin. The range of the steps, controlled by the DC voltage, are from 0dB to -78dB. Each gain step corresponds to a specific input voltage range, as shown in table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and internal clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in volume control graph. For highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gain levels are 1dB/step from 0dB to -6dB, 2dB/step from -6dB to -52dB, and the last step at -78dB as mute mode.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (10)$$

Where :

$$P_O = \frac{V_{ORMS} \times V_{ORMS}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{ORMS} = \frac{V_P}{\sqrt{2}} \quad (11)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (12)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \quad (13)$$

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.2	26.67	0.15	2.00	0.55
0.50	41.67	0.24	2.83	0.7
1.00	58.82	0.34	4.00	0.7
1.3	68.42	0.38	4.47	0.6

**High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 5-V/8Ω BTL Systems

Table 1 calculates efficiencies for four different output power levels when load is 8Ω.

The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

Application Information (Cont.)

BTL Amplifier Efficiency (Cont.)

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation14 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \qquad (14)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \qquad (15)$$

Since the APA4838 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA4838 does not require extra heatsink. The power dissipation from equation15, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation16:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \qquad (16)$$

For TSSOP-28 package with and without thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W and 50°C/W, respectively.

Since the maximum junction temperature ($T_{J,MAX}$) of APA4838 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation16. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Consideration

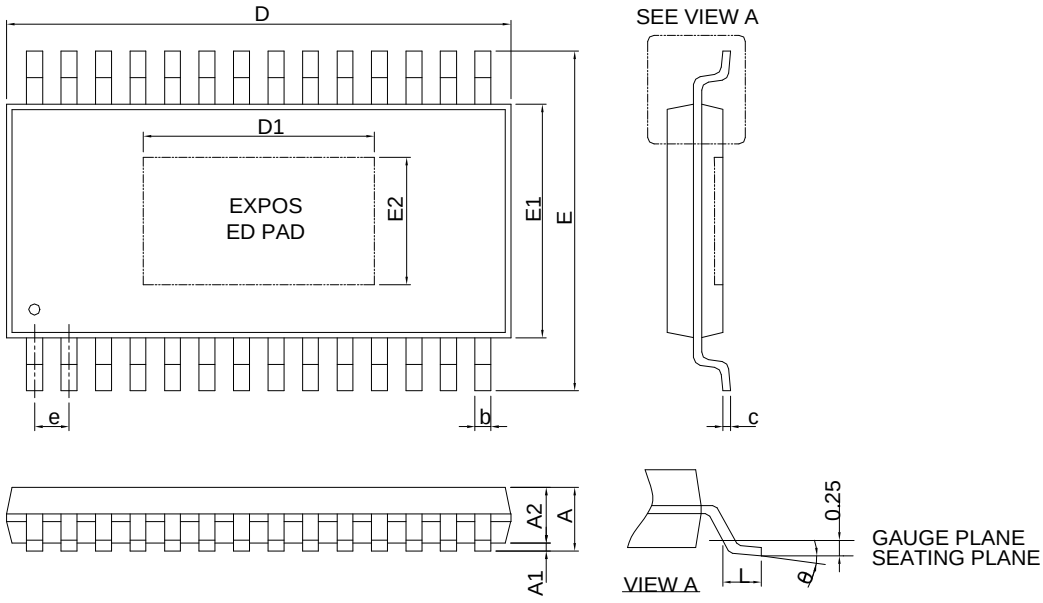
The thermal pad must be connected to the ground. The package with thermal pad of the APA4838 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA4838 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA4838 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA4838 junction temperature below the thermal shutdown temperature (150°C).

Package Information

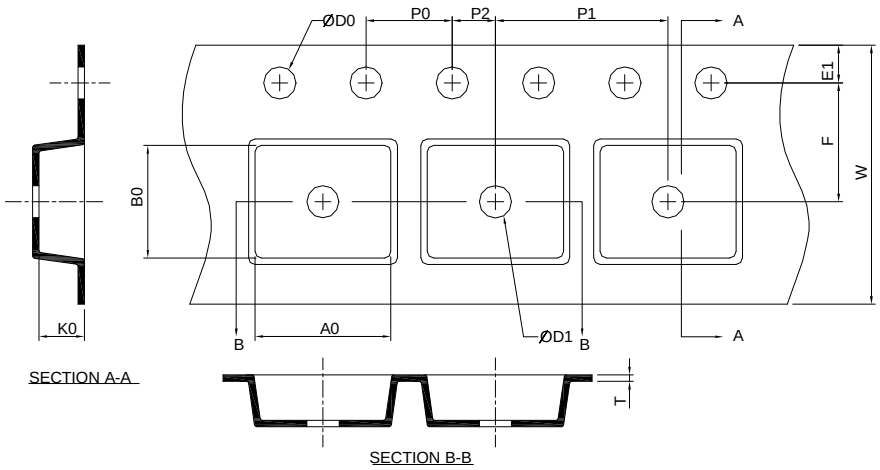
TSSOP-28P

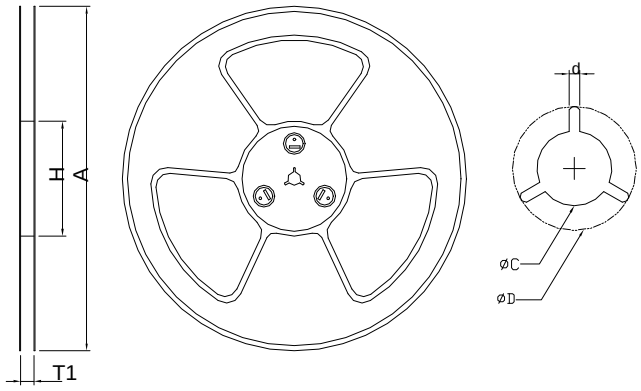


SYMBOL	TSSOP-28P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
D1	4.50	6.00	0.177	0.236
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC MO-153 AET.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TSSOP-28P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.9±0.20	10.20.±0.20	1.50±0.20

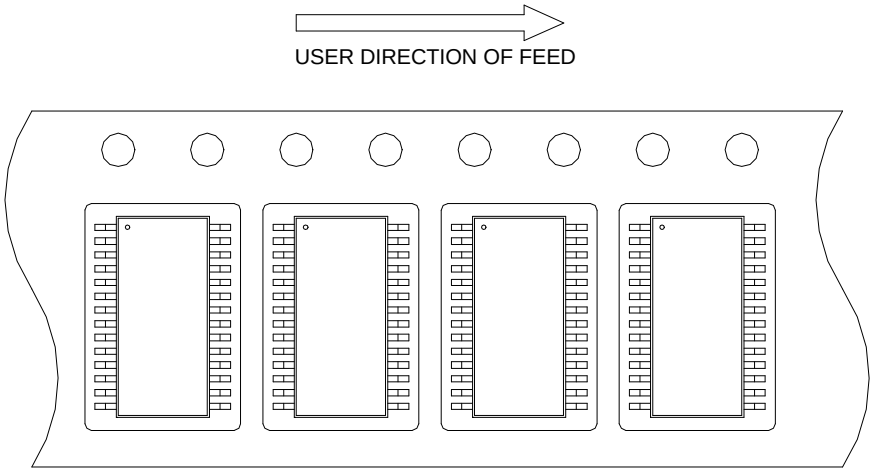
(mm)

Devices Per Unit

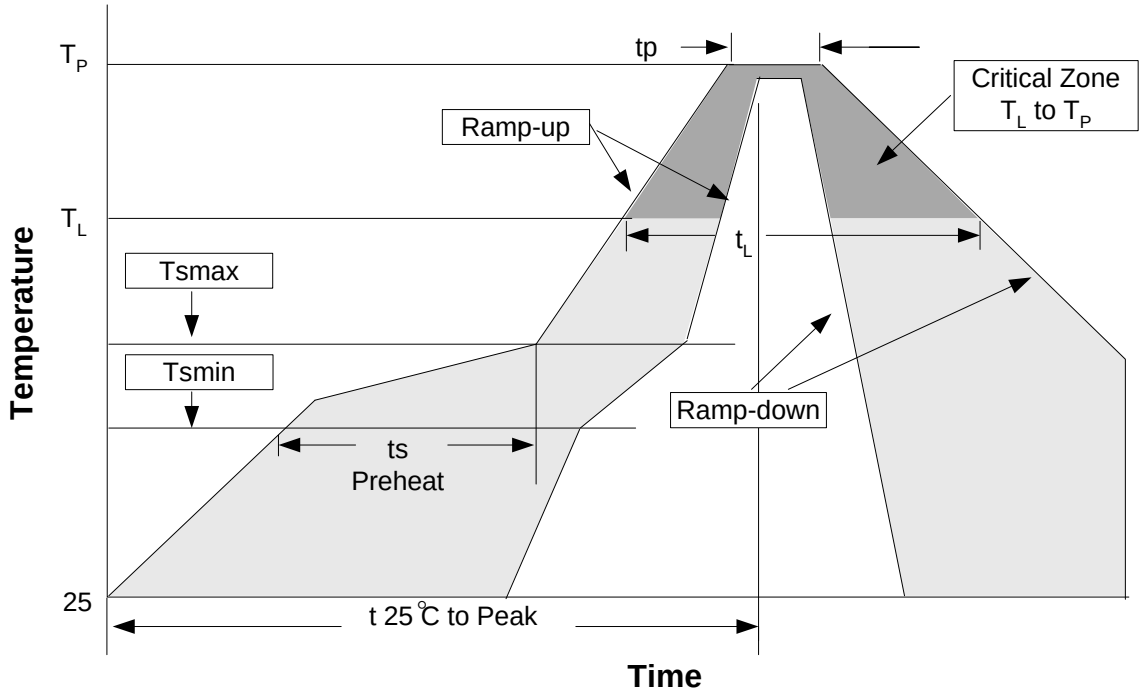
Package Type	Unit	Quantity
TSSOP- 28P	Tape & Reel	2000

Taping Direction Information

TSSOP-28P



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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