Document No. : 031-MP24AD-03

APPROVAL SHEET

Product	Battery Protect Solution IC
Product code	**MP24AD** (001-MP24AD-00)
Production Form	TEP - 5L,BD54
The number of copies	4 copies (1copies return to us)
Date of Registration	September. 07. 2009

Approved By Customer :

Issued	Checked	Approved
H.M Jo	S.W Park	Y.S Kim
02/11	02/11	02/12

ITM

Room 2504 International Science & Technology Building,
Shen Nan Middle Road,Futian,Shen Zhen
TEL:+86-0755-83957788 / +86-0755-82566617
FAX:+86-0755-23919567
E-mail:li@itm-cn.com

■ Contents

■ Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process.
- The charger section can be connected up to absolute maximum rating 28V.

② Detection voltage precision
- Overcharge detection voltage
  ±25mV (Ta=25℃), ±45mV (Ta=-30~70℃)
- Overdischarge detection voltage
  ±70mV (Ta=25℃), ±80mV (Ta=-30~70℃)
- Discharging overcurrent detection voltage
  ±10mV (Ta=25℃), ±20mV (Ta=-30~70℃)
- Charging overcurrent detection voltage
  ±20mV (Ta=25℃), ±40mV (Ta=-30~70℃)

③ Built-in detection delay times
- Overcharge detection delay time
  1.00±0.20s (Ta=25℃), 1.00[+0.50,－0.40]s (Ta=-30~70℃)
- Overdischarge detection delay time)
  96.0±19.2ms (Ta=25℃), 96.0[+48,－38.4]ms (Ta=-30~70℃)
- Discharging overcurrent detection delay time)
  12.0±2.4ms (Ta=25℃), 12.0[+6,－4.8]ms (Ta=-30~70℃)
- Charging overcurrent detection delay time)
  6.0±1.2ms (Ta=25℃), 6.0[+3.0,－2.4]ms (Ta=-30~70℃)
- Short detection delay time)
  400[+160,－120]µs (Ta=25℃), 400[+400,－200]µs (Ta=-30~70℃)

④ With abnormal charger has an ability to detect function
⑤ 0V charge function allowed
⑥ Auto Wake-up function allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.
② The protection for ESD
③ Common drain configuration
④ General characteristics
- V_{DS} (V) = 24V
- I_D (A) = 7A
- $R_{SS(ON)}$ < 44mΩ (V_{GS} = 4.5V, I_D = 5A)
- ESD Rating : 2000V HBM

■ Outline

This is a battery protect solution IC which is integrated with built-in the protection IC to use a lithium ion/lithium polymer secondary batteries developed for 1-cell series and Dual-Nch MOSFET. It functions to protect the battery by detecting overcharge, overdischarge, discharge overcurrent, charge overcurrent and other abnormalities as turning off internal Nch MOSFET. The protection IC is composed of four voltage detectors, short detection circuit, reference voltage sources, oscillator, counter circuit and logical circuits.

The C_{OUT} pin (charge FET control pin) and D_{OUT} pin (discharge FET control pin) outputs are CMOS output, and can drive the internal Nch MOSFET directly. The C_{OUT} output becomes low level after delay time fixed in the IC if overcharge is detected. The D_{OUT} output becomes low level after delay time fixed in the IC if overdischarge, discharge overcurrent or short is detected.

On overcharge state, if the V_{DD} voltage is less than the overcharge release voltage, the C_{OUT} output becomes high level after delay time fixed in the IC. On overdischarge state, if the voltage of the battery rises more than the overdischarge detection voltage with connecting the charger, the D_{OUT} output becomes high level after delay time fixed in the IC. Charging current can be supplied to the battery discharged up to 0V.

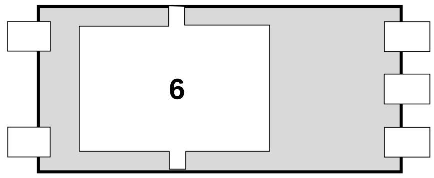
Once discharge overcurrent or short have been detected, if the state of discharge overcurrent or short is released by opening the loads, the D_{OUT} output becomes high level after delay time fixed in the IC. On overdischarge state, the supply current is reduced as less as possible. Once charge overcurrent has been detected, the state of charge overcurrent is released by opening the charger and setting the load.

■ Pin Assignment

[Package: TEP-5L]

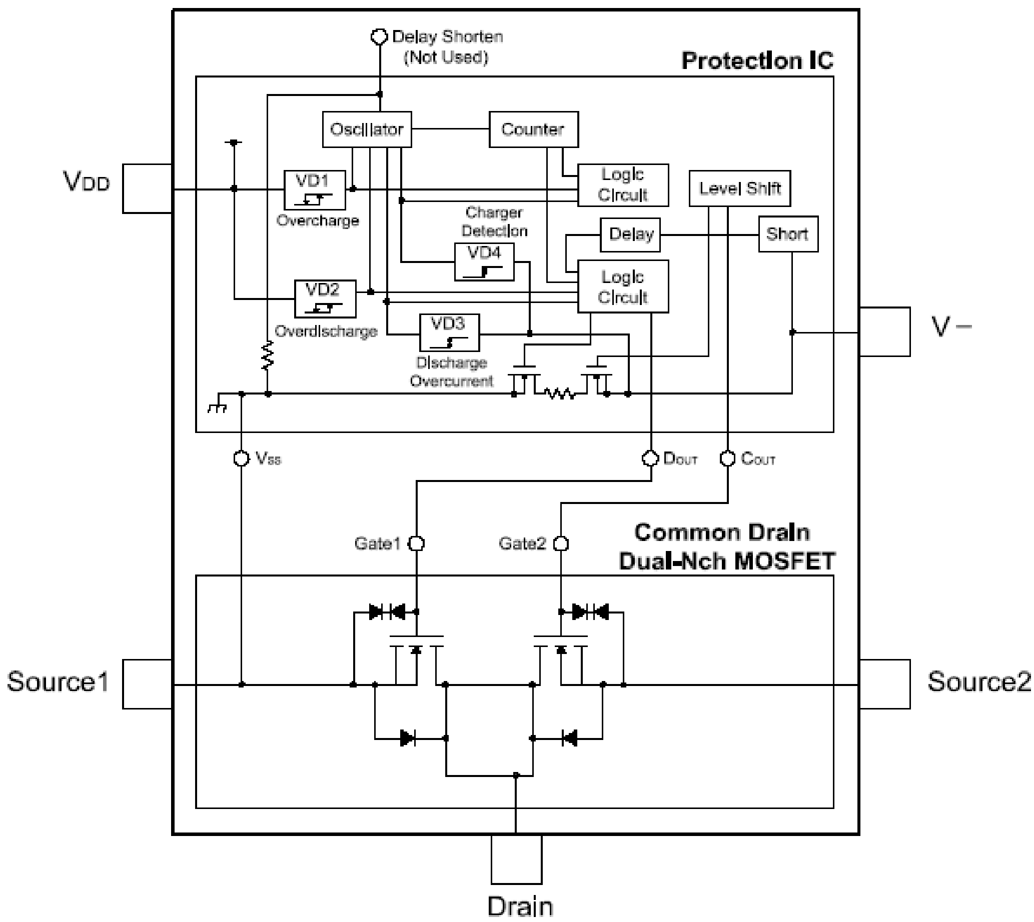
<Top view>

<Bottom view>



1	N.C
2	Source 1(same as V_{SS})
3	Source 2
4	V_{DD}
5	V–
6	Drain

■ Block Diagram



■ Absolute Maximum Rating

※ T_{OPR}=25℃, Source1(V_{SS})=0V

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	−0.3 ~ 12	V
V− Terminal Input Voltage	V−	V_{DD}−28 ~ V_{DD}+0.3	V
DS Terminal Input Voltage	V_{DS}	V_{SS}−0.3 ~ V_{DD}+0.3	V
C_{OUT} Terminal Output Voltage	V_{COUT}	V_{DD}−28 ~ V_{DD}+0.3	V
D_{OUT} Terminal Output Voltage	V_{DOUT}	V_{SS}−0.3 ~ V_{DD}+0.3	V
Operation Temperature	T_{OPR}	−40 ~ +85	℃
Storage Temperature	T_{STG}	−55 ~ +125	℃
Drain−Source Voltage	V_{DS}	24	V
Gate−Source Voltage	V_{GS}	±12	V

■ Electrical Characteristics

※ T_{OPR}=25℃

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Operating Input Voltage	$V_{DD}1$	V_{DD} − V_{SS}	1.5	−	10.0	V	A
Minimum Operating Voltage for 0V Charging	V_{ST}	V_{DD} − V−, V_{DD}−V_{SS}=0V	−	−	1.2	V	A
Overcurrent Release Resistance	R_{SHORT}	V_{DD}=3.6V, V−=1.0V	30	50	100	kΩ	F
C_{OUT} Pin Nch ON Voltage	$V_{OL}1$	I_{OL}=30㎂, V_{DD}=4.5V	−	0.4	0.5	V	−
C_{OUT} Pin Pch ON Voltage	$V_{OH}1$	I_{OH}=−30㎂, V_{DD}=3.9V	3.4	3.7	−	V	−
D_{OUT} Pin Nch ON Voltage	$V_{OL}2$	I_{OL}=30㎂, V_{DD}=2.0V	−	0.2	0.5	V	−
D_{OUT} Pin Pch ON Voltage	$V_{OH}2$	I_{OL}=−30㎂, V_{DD}=3.9V	3.4	3.7	−	V	−
Current Consumption	I_{DD}	V_{DD}=3.9V, V−=0V	−	3.0	6.0	㎂	L
Current Consumption at Stand−By	I_S	V_{DD}=2.0V	−	−	0.5	㎂	L
Overcharge Detection Voltage	$V_{DET}1$	R1=1.0kΩ	4.200	4.225	4.250	V	B
Overcharge Release Voltage	$V_{REL}1$	R1=1.0kΩ	3.985	4.025	4.065	V	B
Overdischarge Detection Voltage	$V_{DET}2$	V−=0V, R1=1.0kΩ	2.430	2.500	2.570	V	D
Overdischarge Release Voltage	$V_{REL}2$	R1=1.0kΩ	2.800	2.900	3.000	V	D
Overdischarge Release Voltage 2	$V_{REL}2'$	Vchg=4.2V, R1=1.0kΩ, R2=2.2kΩ	2.430	2.520	2.610	V	D

※ T_{OPR}=25℃

Item	Symbol	Measure Condition		Min.	Typ.	Max.	Unit	*1
Discharging Overcurrent Detection Voltage	$V_{DET}3$	V_{DD}=3.0V, R2=2.2㏀		0.140	0.150	0.160	V	F
Charging Overcurrent Detection Voltage	$V_{DET}4$	V_{DD}=3.5V, R2=2.2㏀		-0.170	-0.150	-0.130	V	G
Short Detection Voltage	V_{SHORT}	V_{DD}=3.0V		V_{DD}-1.2	V_{DD}-0.9	V_{DD}-0.6	V	F
Overcharge Detection Delay Time	$tV_{DET}1$	V_{DD}=3.6V→4.6V		0.80	1.00	1.20	s	B
Overcharge Release Delay Time	$tV_{REL}1$	V_{DD}=4.6V→3.6V		1.6	2.0	2.4	ms	B
Overdischarge Detection Delay Time	$tV_{DET}2$	V_{DD}=3.6V→2.2V		76.8	96.0	115.2	ms	D
Overdischarge Release Delay Time	$tV_{REL}2$	V_{DD}=2.2V→3.6V		3.2	4.0	4.8	ms	E
Discharging Overcurrent Detection Delay Time	$tV_{DET}3$	V_{DD}=3.0V, V-=0V→1V		9.6	12.0	14.4	ms	F
Discharging Overcurrent Release Delay Time	$tV_{REL}3$	V_{DD}=3.0V, V-=3V→0V		3.2	4.0	4.8	ms	F
Charging Overcurrent Detection Delay Time	$tV_{DET}4$	V_{DD}=3.5V, V-=0V→-1V		4.8	6.0	7.2	ms	G
Charging Overcurrent Release Delay Time	$tV_{REL}4$	V_{DD}=3.5V, V-=-1V→0V		3.2	4.0	4.8	ms	G
Short Detection Delay Time	t_{SHORT}	V_{DD}=3.0V, V-=0V→3.0V		280	400	560	㎲	F
Over Voltage Charger Detection Voltage	Vchg1	V_{DD}=3.6V, R2=2.2㏀		6.0	8.0	10.0	V	A
Over Voltage Charger Release Voltage	Vchg2	V_{DD}=3.6V, R2=2.2㏀		5.3	7.3	9.3	V	A
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250㎂, V_{GS}=0V		24	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V		-	-	1	㎂	
			T_J=55℃	-	-	5		
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±10V		-	-	10	㎂	
Gate-Source Breakdown Voltage	BV_{GSO}	V_{DS}=0V, I_G=±250㎂		±12	-	-	V	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250㎂		0.6	1.0	1.5	V	
Static Source-Source ON-Resistance	$R_{SS(ON)}$	V_{GS}=10V, I_D=5A		-	32	39	mΩ	
			T_J=125℃	-	50	60		
		V_{GS}=4.5V, I_D=5A		-	38	44	mΩ	
		V_{GS}=3.9V, I_D=5A		-	39	45	mΩ	
		V_{GS}=2.5V, I_D=3A		-	50	64	mΩ	
Diode Forward Voltage	V_{SD}	I_S=2A, V_{GS}=0V		0.50	0.69	0.90	V	
Maximum Body-Diode Continuous Current	I_S					4.5	A	

Note : *1 The test circuit symbols.
*2 The parameter is guaranteed by design.

※ T_{OPR}=-30~70℃ *2

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Overcharge Detection Voltage	$V_{DET}1$	R1=1.0kΩ	4.180	4.225	4.270	V	B
Overcharge Release Voltage	$V_{REL}1$	R1=1.0kΩ	3.955	4.025	4.095	V	B
Overdischarge Detection Voltage	$V_{DET}2$	V−=0V, R1=1.0kΩ	2.420	2.500	2.580	V	D
Overdischarge Release Voltage	$V_{REL}2$	R1=1.0kΩ	2.790	2.900	3.010	V	D
Discharging Overcurrent Detection Voltage	$V_{DET}3$	V_{DD}=3.0V, R2=2.2kΩ	0.130	0.150	0.170	V	F
Charging Overcurrent Detection Voltage	$V_{DET}4$	V_{DD}=3.5V, R2=2.2kΩ	−0.190	−0.150	−0.110	V	G
Short Detection Voltage	V_{SHORT}	V_{DD}=3.0V	V_{DD}−1.2	V_{DD}−0.9	V_{DD}−0.6	V	F
Overcharge Detection Delay Time	$tV_{DET}1$	V_{DD}=3.6V→4.6V	0.60	1.00	1.50	s	B
Overcharge Release Delay Time	$tV_{REL}1$	V_{DD}=4.6V→3.6V	1.2	2.0	3.0	ms	B
Overdischarge Detection Delay Time	$tV_{DET}2$	V_{DD}=3.6V→2.2V	57.6	96.0	144.0	ms	D
Overdischarge Release Delay Time	$tV_{REL}2$	V_{DD}=2.2V→3.6V	2.4	4.0	6.0	ms	E
Discharging Overcurrent Detection Delay Time	$tV_{DET}3$	V_{DD}=3.0V, V−=0V→1.0V	7.2	12.0	18.0	ms	F
Discharging Overcurrent Release Delay Time	$tV_{REL}3$	V_{DD}=3.0V, V−=3V→0V	2.4	4.0	6.0	ms	F
Charging Overcurrent Detection Delay Time	$tV_{DET}4$	V_{DD}=3.5V, V−=0V→−1V	3.6	6.0	9.0	ms	G
Charging Overcurrent Release Delay Time	$tV_{REL}4$	V_{DD}=3.5V, V−=−1V→0V	2.4	4.0	6.0	ms	G
Short Detection Delay Time	t_{SHORT}	V_{DD}=3.0V, V−=0V→3.0V	200	400	800	μs	F
Over Voltage Charger Detection Voltage	Vchg1	V_{DD}=3.6V, R2=2.2kΩ	6.0	8.0	10.0	V	A
Over Voltage Charger Release Voltage	Vchg2	V_{DD}=3.6V, R2=2.2kΩ	5.3	7.3	9.3	V	A

Note : *1 The test circuit symbols.
*2 The parameter is guaranteed by design.

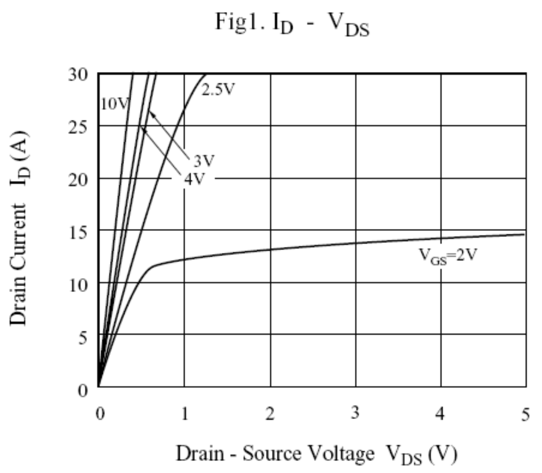


Fig1. I_D - V_{DS}
Drain Current I_D (A)
Drain - Source Voltage V_{DS} (V)
10V
2.5V
3V
4V
V_{GS}=2V

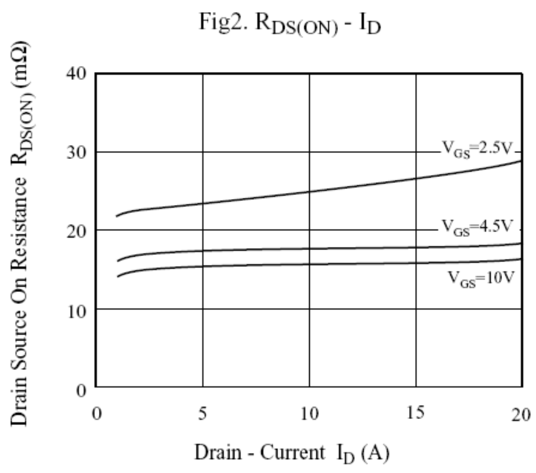


Fig2. $R_{DS(ON)}$ - I_D
Drain Source On Resistance $R_{DS(ON)}$ (mΩ)
Drain - Current I_D (A)
V_{GS}=2.5V
V_{GS}=4.5V
V_{GS}=10V

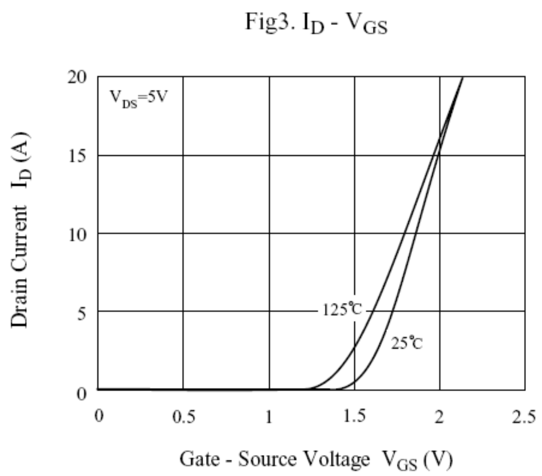


Fig3. I_D - V_{GS}
Drain Current I_D (A)
Gate - Source Voltage V_{GS} (V)
V_{DS}=5V
125℃
25℃

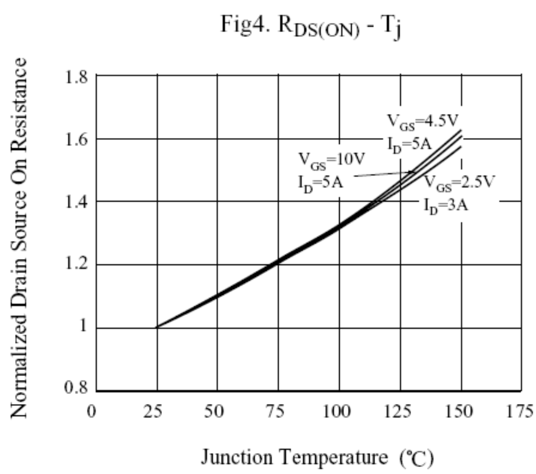


Fig4. $R_{DS(ON)}$ - T_j
Normalized Drain Source On Resistance
Junction Temperature (℃)
V_{GS}=4.5V
I_D=5A
V_{GS}=10V
I_D=5A
V_{GS}=2.5V
I_D=3A

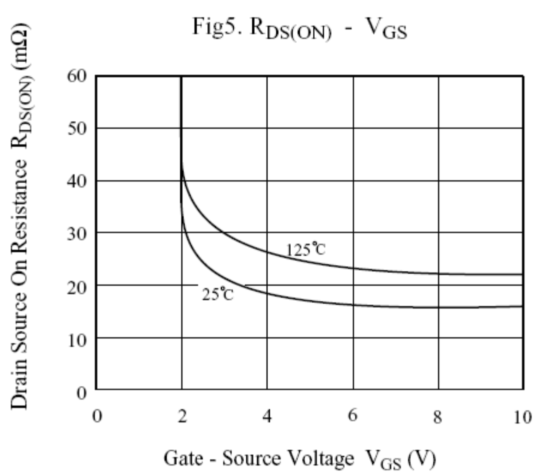


Fig5. $R_{DS(ON)}$ - V_{GS}
Drain Source On Resistance $R_{DS(ON)}$ (mΩ)
Gate - Source Voltage V_{GS} (V)
125℃
25℃

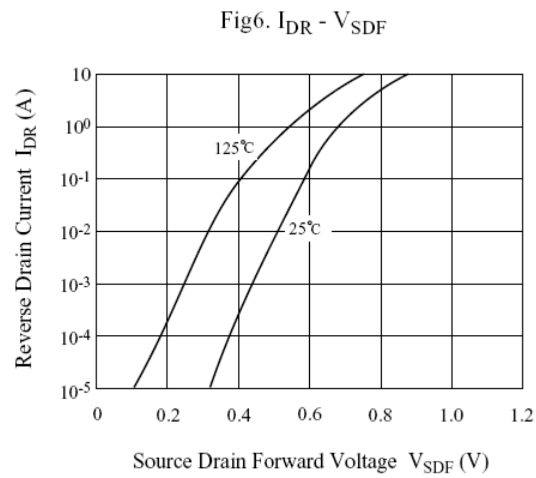


Fig6. I_{DR} - V_{SDF}
Reverse Drain Current I_{DR} (A)
Source Drain Forward Voltage V_{SDF} (V)
125℃
25℃

Fig7. V_{GS} - Q_g

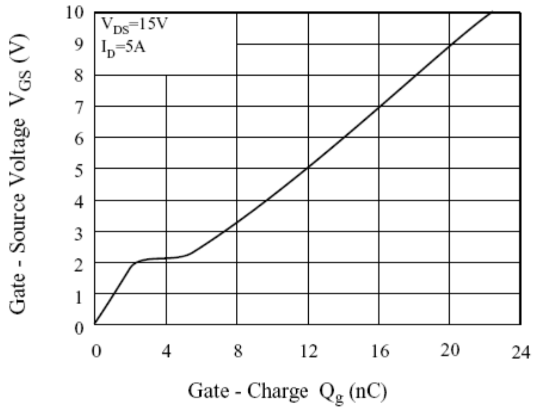
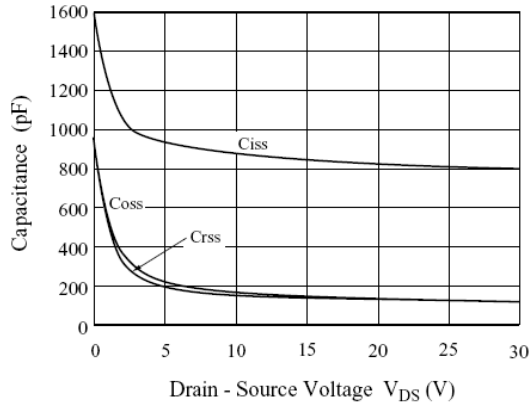
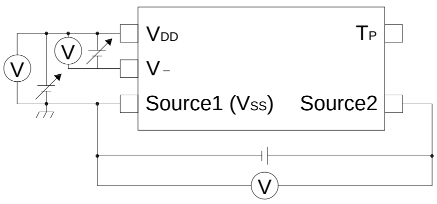


Fig8. C - V_{DS}

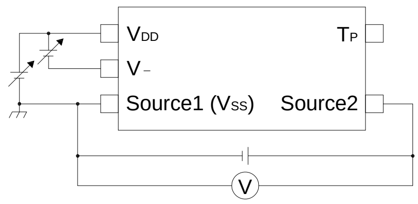


■ Measuring Circuit

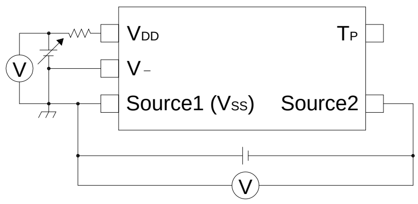
A.



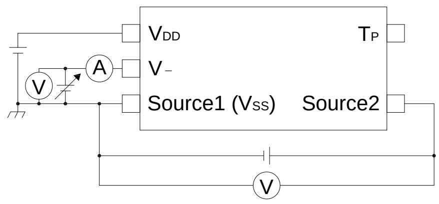
E.



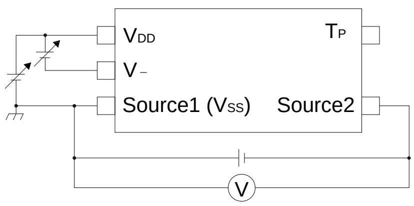
B.



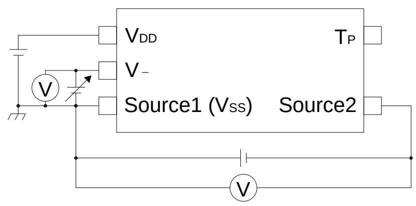
F.



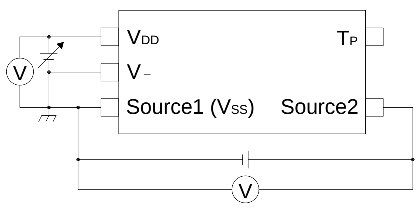
C.



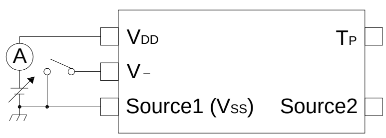
G.



D.



H.



■ Operation

1. Overcharge detector (VD1)

The VD1 monitors V_{DD} pin voltage during charge. In the state of charging the battery, it will detect the overcharge state of the battery if the V_{DD} terminal voltage becomes higher than the overcharge detection voltage(Typ. 4.225V). And then the C_{OUT} terminal turns to low level, so the internal charging control Nch MOSFET turns OFF and it forbids to charge the battery.

After detecting overcharge, it will release the overcharge state if the V_{DD} terminal voltage becomes lower than the overcharge release voltage(Typ.4.025V). And then the C_{OUT} terminal turns to high level, so the internal charging control Nch MOSFET turns ON, and it accepts to charge the battery.

When the V_{DD} terminal voltage is higher than the overcharge detection voltage, to disconnect the charger and connect the load, leave the C_{OUT} terminal low level, but it accepts to conduct load current via the paracitical body diode of the internal Nch MOSFET. And then if the V_{DD} terminal voltage becomes lower than the overcharge detection voltage, the C_{OUT} terminal turns to high level, so the internal Nch MOSFET turn ON, and it accepts to charge the battery.

The overcharge detection and release have delay time decided internally. When the V_{DD} terminal voltage becomes higher than the overcharge detection voltage, if the V_{DD} terminal voltage becomes lower than the overcharge detection voltage again within the overcharge detection delay time(Typ. 1.00s), it will not detect overcharge. And in the state of overcharge, when the V_{DD} terminal voltage becomes lower than the overcharge release voltage, if the V_{DD} terminal voltage backs higher than the overcharge release voltage again within the overcharge release delay time(Typ. 2ms), it will not release overcharge.

The output driver stage of the C_{OUT} terminal includes a level shifter, so it will output the V_- terminal voltage as low level. The output type of the C_{OUT} terminal is CMOS output between V_{DD} and V_- terminal voltage.

2. Overdischarge detector (VD2)

The VD2 monitors V_{DD} pin voltage during discharge. In the state of discharging the battery, it will detect the overdischarge state of the battery if the V_{DD} terminal becomes lower than the overdischarge detection voltage (Typ. 2.500V). And then the D_{OUT} terminal turns to low level, so the internal discharging control Nch MOSFET turn OFF and it forbids to discharge the battery.

Once overdischarge has been detected, overdischarge is released and the D_{OUT} output becomes high level, if the voltage of the battery rises more than the overdischarge detection voltage with connecting the charger, or more than the overdischarge release voltage without connecting the charger. Charging current is supplied through a parasitic diode of Nch MOS FET when the V_{DD} terminal voltage is below the overdischarge detection voltage to the connection of the charger, and the D_{OUT} terminal enters the state which can be discharged by becoming high level,and turning on Nch MOS FET when the V_{DD} terminal voltage rises more than the overdischarge detection voltage.

When the battery voltage is about 0V, if the charger voltage is higher than the minimum operating voltage for 0V charging (Max. 1.2V), the C_{OUT} terminal outputs high level and it accepts to conduct charging current.

The overdischarge detection have delay time decided internally. When the V_{DD} terminal voltage becomes lower than the overdischarge detection voltage, if the V_{DD} terminal voltage becomes higher than the overdischarge detection voltage again within the overdischarge detection delay time (Typ. 96ms), it will not detect overdischarge. Moreover, the overdischarge release delay time (Typ. 4ms) exists, too.

All the circuits are stopped, and after the overdischarge is detected, it is assumed the state of the standby, and decreases the current (standby current) which IC consumes as much as possible. (When V_{DD}=2V, Max. 0.5uA).

The output type of the D_{OUT} terminal is CMOS output between V_{DD} and V_{SS} terminal voltage.

3. Discharge overcurrent detector, Short detector (VD3, Short Detector)

In the state of chargable and dischargabe, VD3 monitors the voltage level of V_- pin. If the V_- terminal voltage becomes higher than the discharging overcurrent detection voltage (Typ. 0.150V) by short of loads, etc., it will detect discharging overcurrent state. If the V_- terminal voltage becomes higher then short detection voltage (Typ. V_{DD}−0.9V), it will detect discharging overcurrent state, too. And then the D_{OUT} terminal outputs low level, so the internal discharging control Nch MOSFET turns OFF, and it protects from large current discharging.

The discharging overcurrent detection has delay time decided internally. When the V_- terminal voltage becomes higher than the discharging overcurrent detection voltage, if the V_- terminal voltage becomes lower than the discharging overcurrent detection voltage within the discharging overcurrent detection delay time (Typ. 12ms), it will not detect discharging overcurrent. Morever, the discharging overcurrent release delay time (Typ. 4ms) exists, too.

The short detection delay time (Typ. 400us) decided internally exists, too.

The discharging overcurrent release resistance (Typ. 50kohm) is built into between V_- terminal and V_{SS} terminal. In the state of discharging overcurrent or short, if the load is opened, V_- terminal is pulled down to the V_{SS} via the discharging overcurrent release resistance. And when the V_- terminal voltage becomes lower than the discharging overcurrent detection voltage, it will automatically release discahrging overcurrent or short state. if discharging overcurrent or short is detected, the discharging overcurrent release resistance turns ON. On the normal state (chargable and dischargable state), the discharging overcurrent release resistance is OFF.

4. Charge overcurrent detector (VD4)

In the state of chargable and dischargable, VD4 monitors the voltage level of V_- pin. If the V_- terminal voltage becomes lower than charging overcurrent detection voltage (Typ. −0.150V) by abnormal voltage or current charger, etc., it will detect charging overcurrent state. And then the C_{OUT} terminal outputs low level, so the internal charging control Nch MOSFET turn OFF, and it protects from large current charging.

It release charging overcurrent state if the abnormal charger is disconnected and the load is connected.

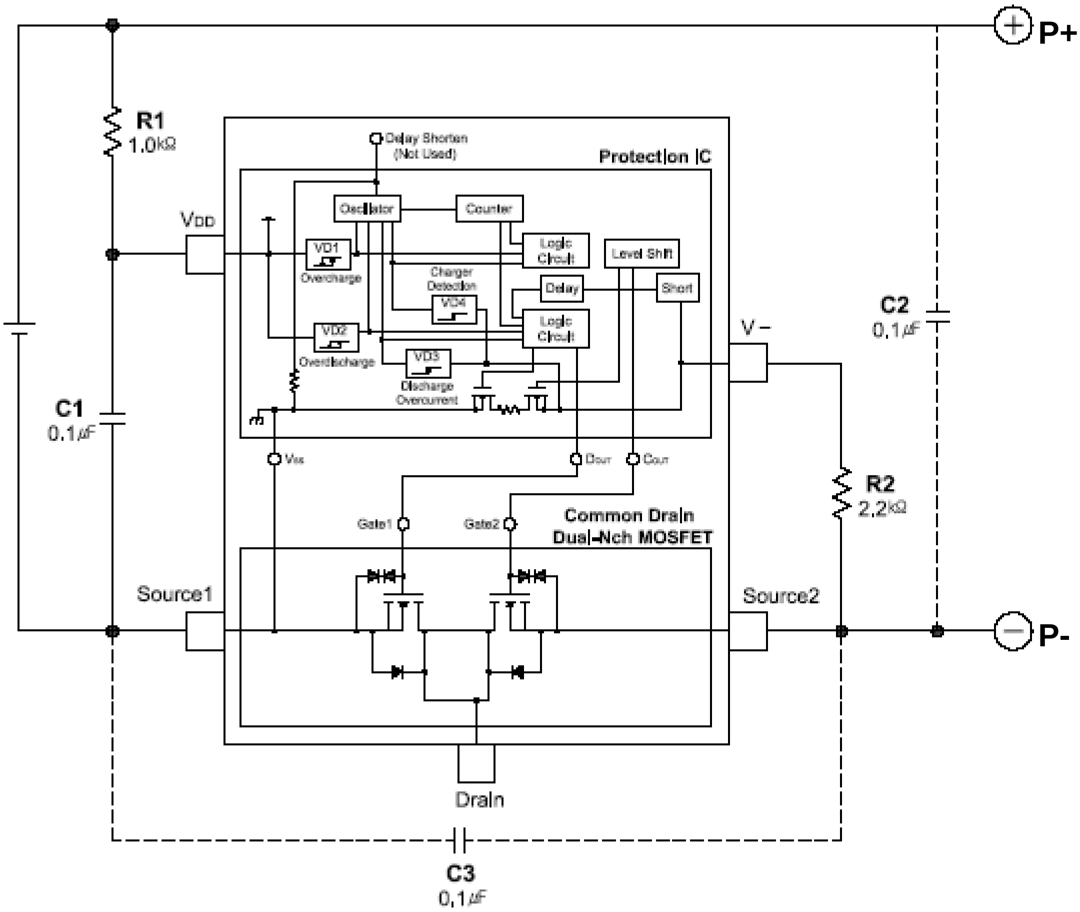
The charging overcurrent detection has delay time decided internally. When the V_- terminal voltage becomes lower than the charging overcurrent detection voltage, if the V_- terminal voltage becomes higher than the charging overcurrent detection voltage within the charging overcurrent detection delay time (Typ. 6ms), it will not detect charging overcurrent. Morever, the charging overcurrent release delay time (Typ. 4ms) exists, too.

5. Over voltage charger detector

By monitoring charger voltage between V_{DD} terminal and V_- terminal, and when the voltage becomes higher than over voltage charger detection voltage (Typ.8.0V), C_{OUT} output becomes low level and internal Nch MOSFET is turned to OFF. And when the voltage becomes lower than over voltage charger release voltage(Typ.7.3V), C_{OUT} output becomes high level and internal Nch MOSFET is turned to ON. Please note that the larger value of R2, the larger detection voltage.

There is no delay time of detection and release for this function.

■ Application Circuit (Example)



※ Application Hint

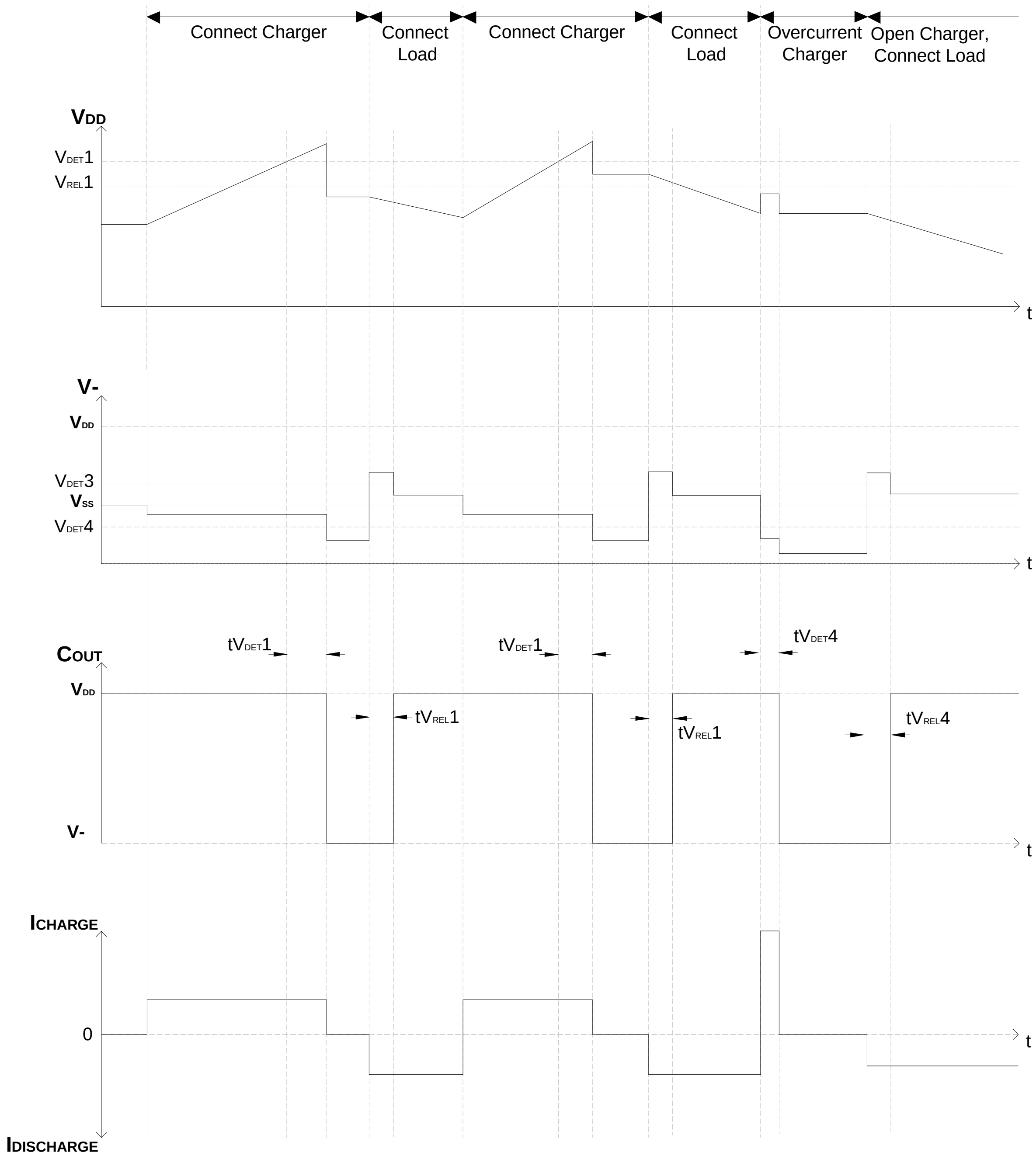
R1 and C1 stabilize a supply voltage ripple. However, the detection voltage rises by the current of penetration in IC of the voltage detection when R1 is enlarged, so the value of R1 is adjusted to 1kohm or less. Moreover, adjust the value of C1 to 0.1uF or more to do the stability operation, please.

R1 and R2 resistors are current limit resistance if a charger is connected reversibly or a highvoltage charger that exceeds the absolute maximum rating is connected. R1 and R2 may cause a power consumption will be over rating of power dissipation, therefore the `R1+R2` should be more than 1kohm. Moreover, if R2 is too enlarged, the charger connection release cannot be occasionally done after the overdischarge is detected, so adjust the value of R2 to 10kohm or less, please.

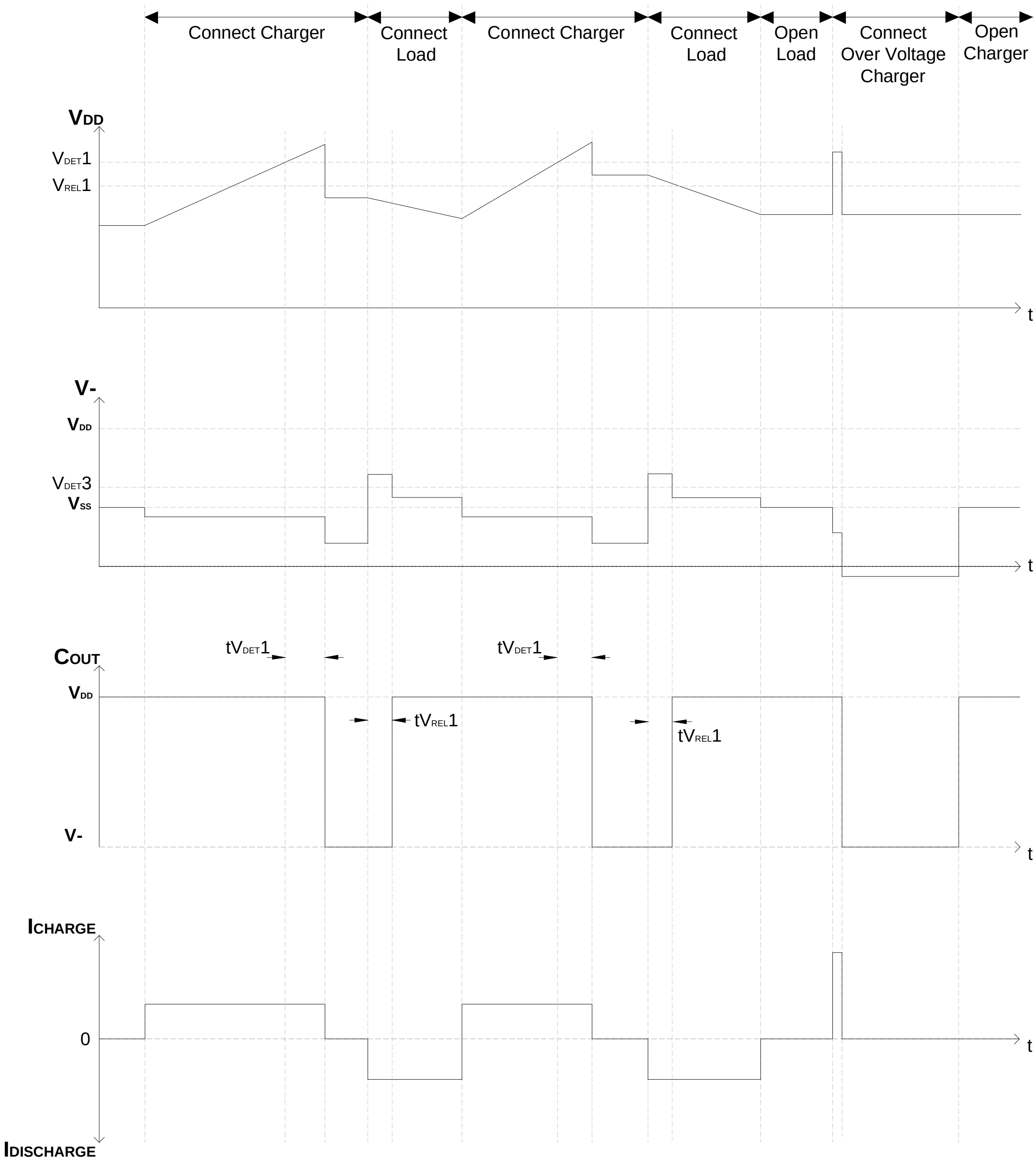
C2 and C3 capacitors have effect that the system stability about voltage ripple or imported noise. After check characteristics, decide that these capacitors should be inserted or not, where should be inserted, and capacitance value, please.

■ Timing Chart

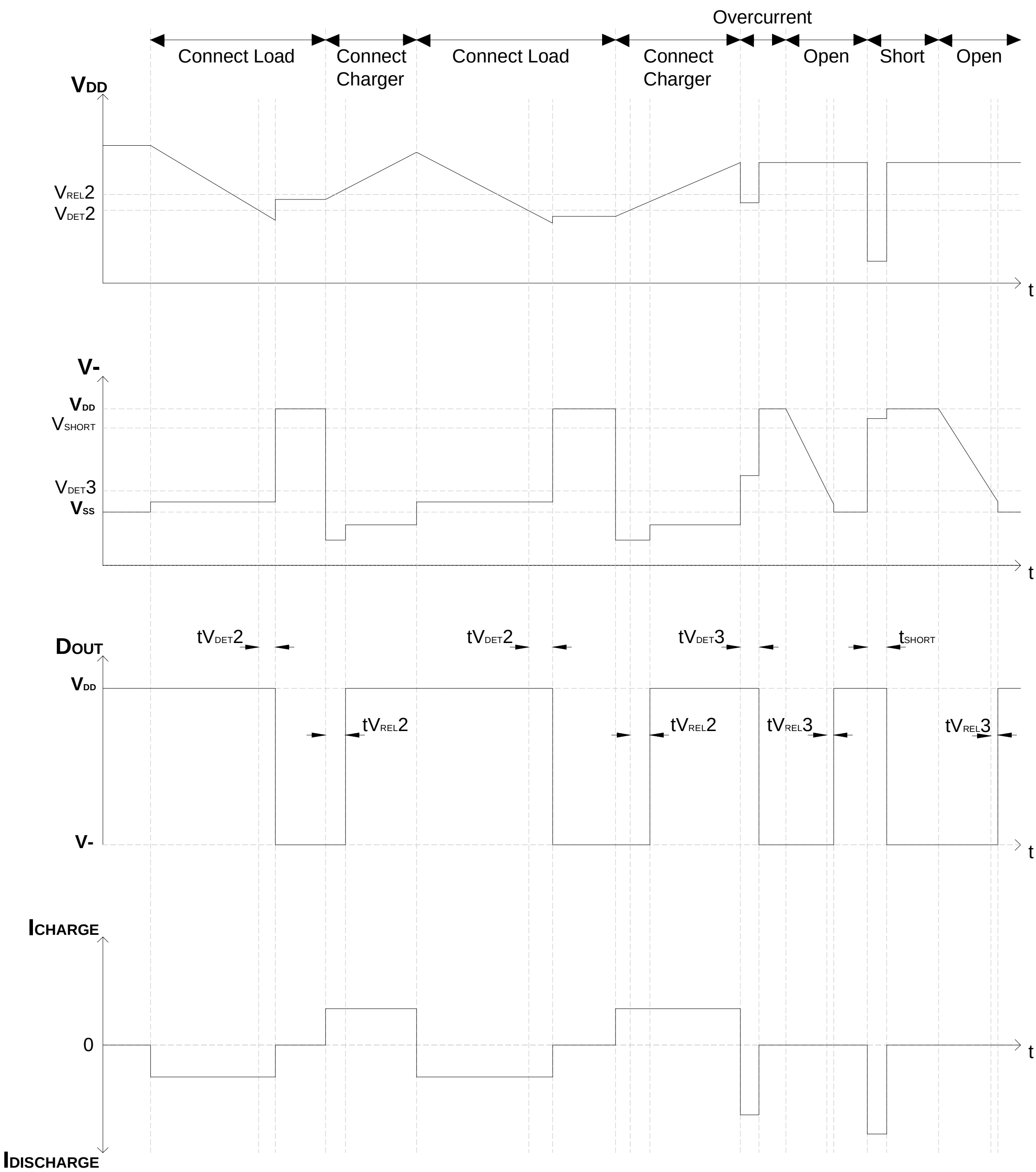
1. Overcharge, Charging overcurrent operations



2. Overcharge, Overvoltage charger operations

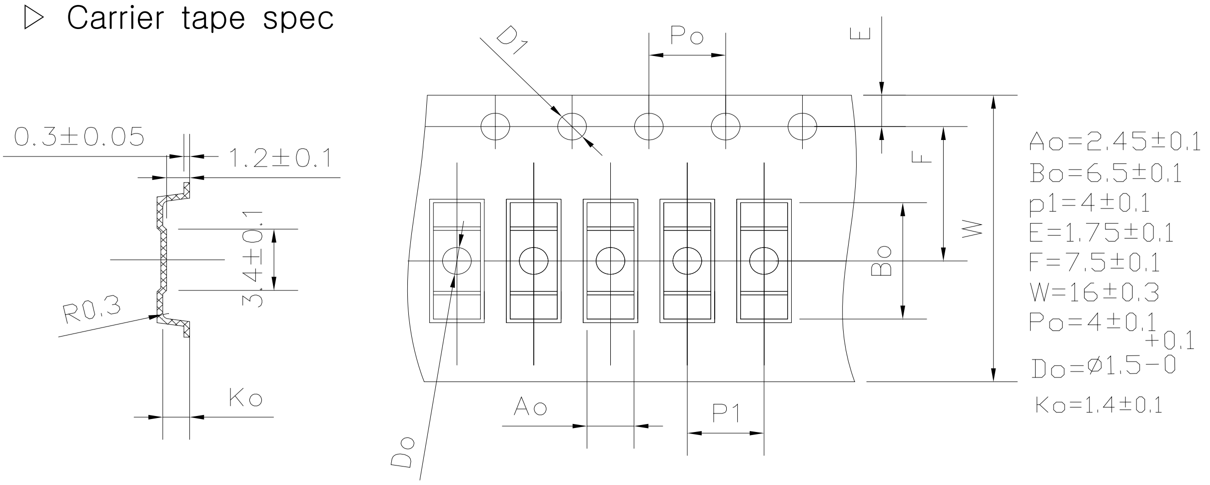


3. Overdischarge, Discharging Overcurrent and Short operations

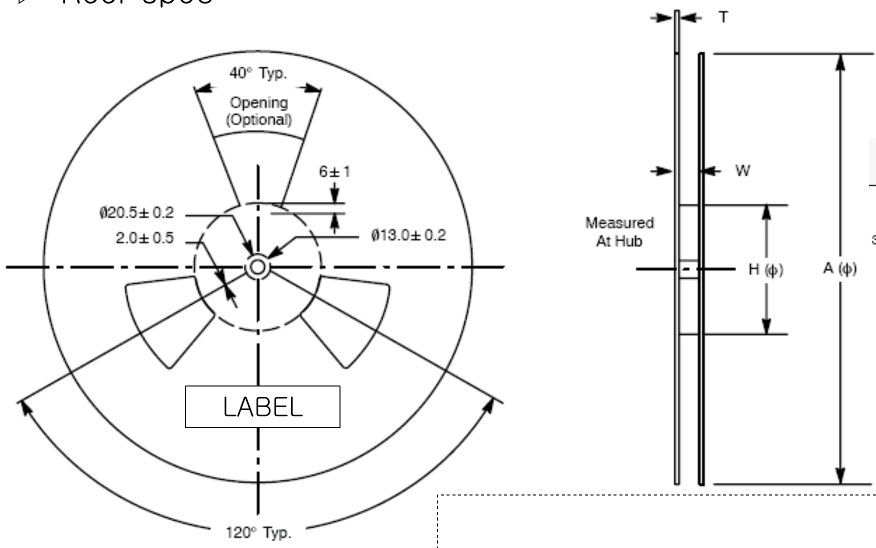


■ Packing spec

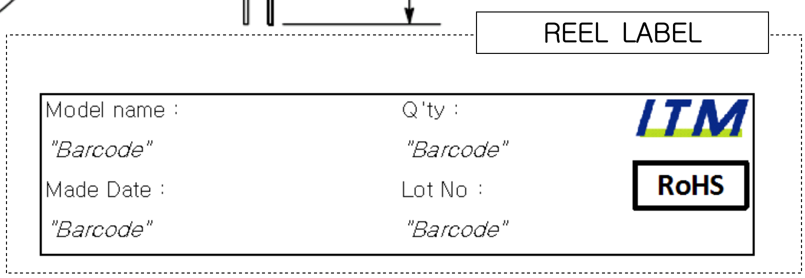
▷ Carrier tape spec



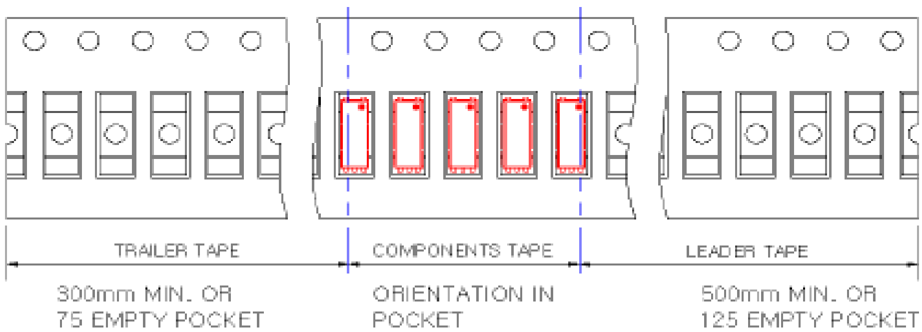
▷ Reel spec



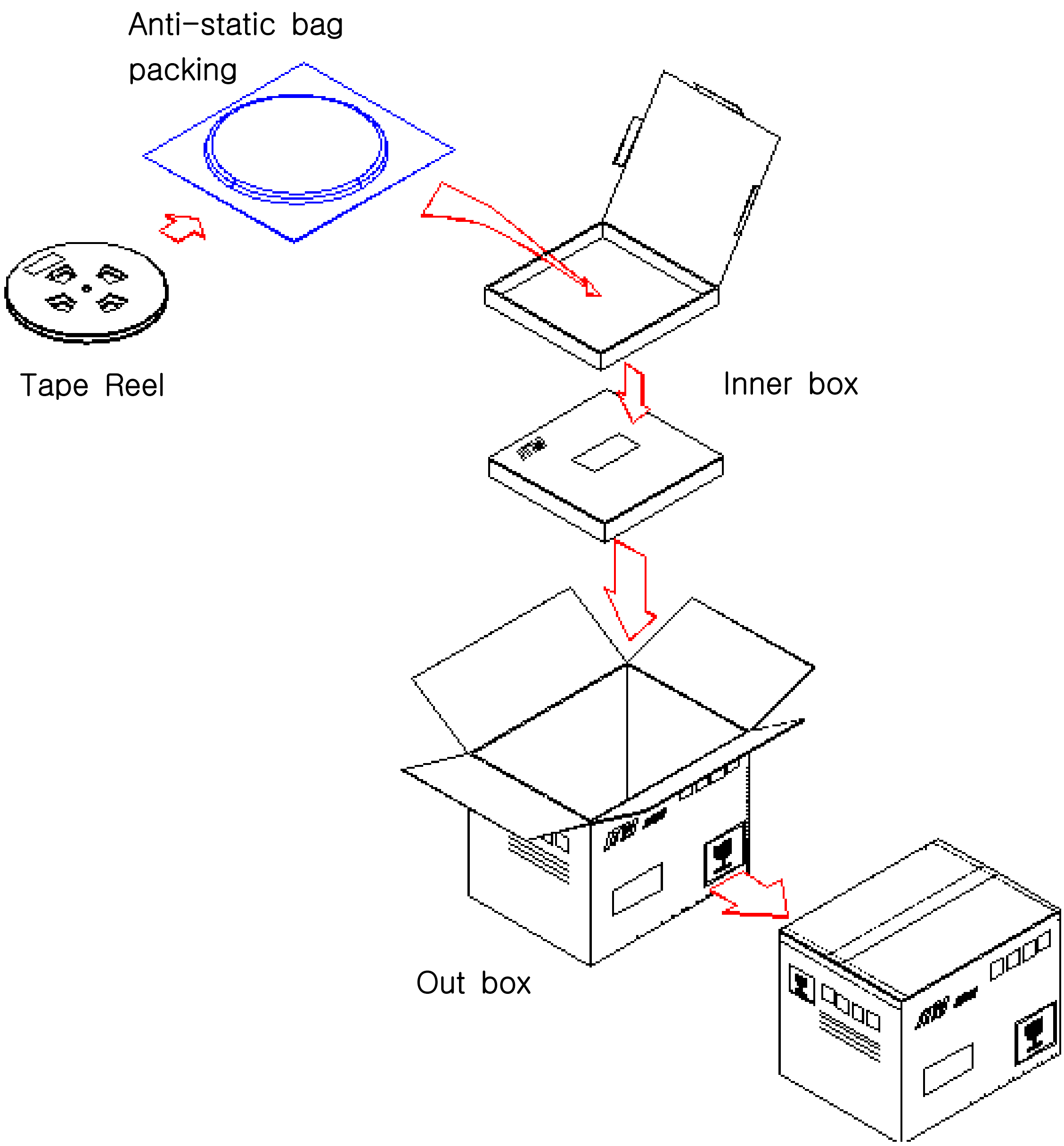
A	W		TAPE WIDTH	H	T
330±2	16.4	+2.0 −0	16	100±1	2.5±0.5



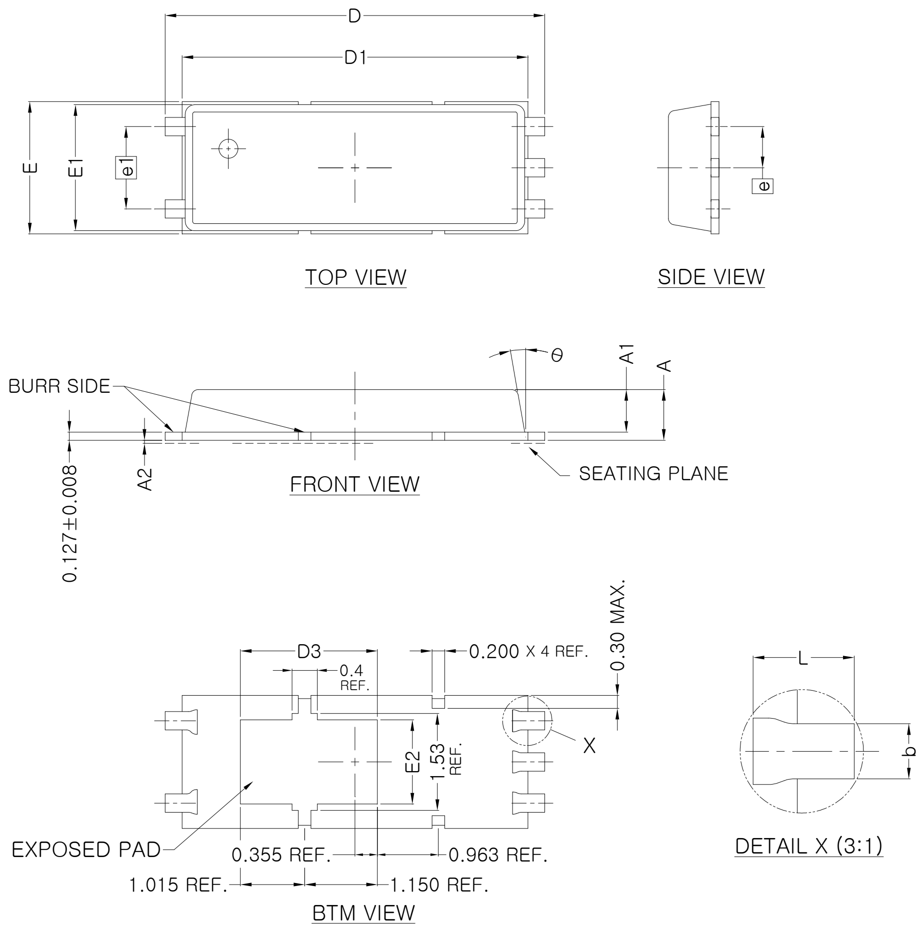
▷ Taping spec



▷ OUTER BOX PACKING SPECIFICATION



■ Package Description



SYMBOL	DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.750	0.800	0.850	
A1	0.623	0.673	0.723	
A2	–	–	0.050	
D	5.900	6.000	6.100	
D1	5.320	5.370	5.420	
D3	2.220 REF.			
E	2.000	2.100	2.200	
E1	1.950	2.000	2.050	
E2	1.330 REF.			
θ	–	–	10 °	
e	0.650 BSC			
e1	1.300 BSC			
L	0.350	–	–	
b	0.255	0.300	0.390	

NOTE

1. LEAD BURR : VERTICAL MAX 0.025
   HORIZONTAL MAX 0.025
   BURR SIDE : ALL TOP SIDE
2. MOLD BURR & FLASH : PACKAGE OUT LINE BURR MAX 0.100
   EXPOSED PAD FLASH MAX 0.200
3. PACKAGE WARPAGE MAX 0.025
4. LEAD AND EXPOSED PAD PLATING : PURE TIN
   THICKNESS> 7.62~25.4um

■ Marking Contents